04/1/02

Re: 09/829,797

Examiner Lewis,

Attached are edited search results from the patent and nonpatent databases.

Red tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Derrick Blalock,
STIC-EIC2800
306-0935
CP4-9C18

(FILE 'HOME' ENTERED AT 14:46:37 ON 01 APR 2002)

FILE 'WPIX, JAPIO' ENTERED AT 14:47:07 ON 01 APR 2002

L1	14672	S	(BOND?)(2N)(PAD OR PADS)
L2	8947	S	(U11-D03A2 OR U11-D03B1)/MC
L3	366784	S	(DIELETRIC OR INSULAT? OR OXIDE)(2N)(FILM OR LAYER? OR COAT#
L4	157901	S	(VIA OR VIAS OR THROUGH OR PATH)(2N)(LINES OR LINE OR WIRE OR
L5	1645106	S	STACK### OR MOUNT? OR PILE OR PILED OR MOUND?
L6	48222	S	TUNGSTEN OR WOLFRAM
L7	10	S	(US2001045669 OR US6215182 OR US6191023 OR US6166443 OR US595
L8	14	S	(TW382812 OR US6239496 OR US6219911 OR US6218728 OR US6191482
L9	18	S	(US5929468 OR EP926721 OR JP11145180 OR JP10341082 OR JP10340
L10	15	S	(US6204162 OR JP2000349088 OR US6144099 OR US6080596 OR JP200
L11	6	S	(US5262354 OR US6300688 OR US6212056 OR JP3046024 OR JP200015
L12	15	S	(US6258715 OR JP2001176874 OR JP2001135639 OR US6180503 OR JP
L13	6	S	(JP06177200 OR US5357136 OR JP02144921 OR US3714521)/PN
L14	84	S	L7-13
L15	754171	S	PARALLEL OR COLLATERAL OR (SIDE(2N)BY(2N)SIDE)
L16	225366	S	(METAL?)(2N)(FILM OR LAYER? OR COAT####)
L17	1	S	US6103554/PN
L18	4863	S	(L1 OR L2) AND L5
L19	374	S	L18 AND L16
L20	118	S	L19 AND L3
L21	8	S	L20 AND L4
L22	7	S	L21 NOT (L14 OR L17)
L23	4	S	L20 AND L15
L24	0	S	L21 NOT (L14 OR L17 OR L22)
L25	19	S	L19 AND L4
L26	10	S	L25 NOT (L14 OR L17 OR L22)
L27	4863	S	L18 AND L5
L28	287	S	L27 AND L4
L29	39	S	L28 AND L3
L30	31	S	L29 NOT (L14 OR L17 OR L22 OR L26)
L31	0	S	L30 AND L15
L32	211	S	L18 AND L15
L33	9	S	L32 AND (METAL?)(2N)(LINE OR WIRE)
L34	8	S	L33 NOT (L14 OR L17 OR L22 OR L26 OR L30)
L35	6	S	L30 AND (METAL?)(2N)(LINE OR WIRE)
L36	25	S	L30 NOT L35
L37	29	S	L18 AND L6
L38	28	S	L37 NOT (L14 OR L17 OR L22 OR L26 OR L30 OR L33 OR L34 OR L
L39	0	S	L38 AND L4

L37 ANSWER 1 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2002-013466 [02] WPIX
DNN N2002-010893 DNC C2002-003650
TI Flip-chip **mounting** structure for semiconductor device such as integrated circuit, has solder layer comprising tin whose concentration reduction is delayed.
DC L03 U11
PA (MATW) MATSUSHITA ELECTRIC WORKS LTD
CYC 1
PI JP 2001217275 A 20010810 (200202)* 9p
ADT JP 2001217275 A JP 2000-26275 20000203
PRAI JP 2000-26275 20000203
AB JP2001217275 A UPAB: 20020109
NOVELTY - A solder bump (5) is provided on a **tungsten** thin film electrode (80) arranged on a ceramic substrate (9). A solder layer (6) comprising Sn is laminated on the solder bump, on which an aluminum electrode (2) is provided through a copper core layer (4). The reduction of density concentration of solder layer is delayed. A chip (1) is **mounted** on the aluminum electrode.
USE - For **mounting** semiconductor device such as integrated circuit.
ADVANTAGE - Since concentration reduction of Sn is delayed, crack initiation due to void formation becomes slow and durability of solder bump's junction portion is prolonged.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of flip-chip **mounting** structure.
Chip 1
Aluminum electrode 2
Copper core layer 4
Solder bump 5
Solder layer 6
Ceramic substrate 9
Tungsten thin film electrode 80
Dwg.1/10

L37 ANSWER 2 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2002-009228 [01] WPIX
CR 2001-389280 [40]
DNN N2002-007669 DNC C2002-002169
TI Direct contact through hole type wafer structure for forming memory modules, includes contact plugs positioned in first silicon substrate and exposed by opening.
DC A85 U11 U12
IN HAN, C; HSUAN, M
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6252300 B1 20010626 (200201)* 14p
ADT US 6252300 B1 US 1999-260218 19990301
PRAI TW 1999-100499 19990114
AB US 6252300 B UPAB: 20020105
NOVELTY - A direct contact through hole type wafer structure includes contact plugs positioned in a first silicon substrate and exposed by an opening.
DETAILED DESCRIPTION - A direct contact through hole type wafer structure comprises a silicon-on-insulator substrate having a first silicon substrate, a second silicon substrate and a first insulation layer with the first insulation layer positioned between the first and second silicon substrates, where at least one opening is formed in the second

silicon substrate and penetrates into the first silicon substrate through the first insulation layer. Device(s) is positioned on the first silicon substrate. Contact plugs (72) are positioned in the first silicon substrate and exposed by the opening. Dielectric layers and patterned conductive layers couple with the device and the contact plugs and plugs in the dielectric layers, and the dielectric layers and the patterned conductive layers (78 a-b) being alternately **stacked** on the first silicon substrate, where **bonding pad**(s) is formed on an uppermost conductive layer and exposed by an uppermost dielectric layer formed on the uppermost conductive layer. A second insulation layer is positioned in the opening, where the second insulation layer is on a surface of the opening and exposes the contact plugs. A barrier layer is positioned on the second insulation layer and coupled with the contact plugs. A metal layer is positioned on the barrier layer.

USE - For forming memory modules.

ADVANTAGE - The invention reduces volume and height of the package. It also reduces signal-transmitting path, and electrical impedance, thus problem of signals delayed and decayed is avoided.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of packages.

Bumps 60

Contact plugs 72

Conductive layers 78a-b

Dwg.3/4

L37 ANSWER 3 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-637795 [73] WPIX
DNN N2001-476627 DNC C2001-188610
TI Flip chip assembly for **mounting** integrated circuit device to substrate, using solder connection between contact member and flip chip.
DC L03 U11
IN BRANDENBURG, S D; DELHEIMER, C I; KOORS, M A; OBERLIN, G E; VAJAGICH, R
PA (DELP-N) DELPHI TECHNOLOGIES INC
CYC 1
PI US 6262489 B1 20010717 (200173)* 6p
ADT US 6262489 B1 US 1999-434552 19991108
PRAI US 1999-434552 19991108
AB US 6262489 B UPAB: 20011211

NOVELTY - A flip chip assembly (10) comprises:

(a) a flip chip (18) **mounted** on a substrate (12);

(b) an electrical contact member (20) above the flip chip;

(c) first and second solder connections (22, 24) connecting the flip chip and the contact member to the substrate, respectively; and

(d) a third solder connection (26) connecting the contact member to an electrical contact on the flip chip.

DETAILED DESCRIPTION - A flip chip assembly comprises:

(i) a flip chip **mounted** on a substrate;

(ii) an electrical contact member above the flip chip; and

(iii) first, second and third solder connections.

The flip chip has an integrated circuit (IC) (28) on its lower surface and an electrical contact on its upper surface, while the contact member has a planar portion (30) and at least two legs (32).

The planar portion has a lower coefficient of thermal expansion (CTE) than the legs.

The first solder connections connect the flip chip to a first conductor (14) on the substrate, while the second solder connections connect the legs of the contact member to a second conductor (16) on the substrate. The third solder connection connects the planar portion of the contact member to the electrical contact on the upper surface of the flip

chip.
An INDEPENDENT CLAIM is also included for a method of attaching a flip chip to a substrate.
USE - For **mounting** a semiconductor IC device to a substrate.
ADVANTAGE - The inventive flip chip assembly provides an uncomplicated method for attaching the IC and the electrical contact to the substrate. The third solder connection draws the flip chip to the contact member during reflow soldering, preventing the first solder connections from collapsing. Thus, a stand-off height between the flip chip and the substrate is provided to enable stress relief during thermal cycles, to allow penetration of cleaning solutions, and to enable the penetration of mechanical bonding and underfill materials (40).
DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional side view of the flip chip assembly.
Flip chip assembly 10
Substrate 12
First conductor 14
Second conductor 16
Flip chip 18
Electrical contact member 20
First solder connections 22
Second solder connections 24
Third solder connection 26
IC 28
First portion 30
Legs 32
Layer of planar portion 34
Heatsink 36
Insulation layer 38
Underfill material 40
Dwg.3/3

L37 ANSWER 4 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-389280 [41] WPIX
CR 2002-009228 [44]
DNN N2001-286311 DNC C2001-118664
TI Direct contact through hole type wafer used for forming a wafer-level package has devices and contacts coupled to each other on both sides of the wafer.
DC A85 L03 U11 U14
IN HAN, T; SHIUAN, M; HAN, C; HSUAN, M C
PA (UNMI-N) UNITED MICROELECTRONICS CORP; (HANC-I) HAN C; (HSUA-I) HSUAN M C
CYC 2
PI US 2001005046 A1 20010628 (200141)* 15p
US 6323546 B2 20011127 (200175)
TW 442873 A 20010623 (200206)
ADT US 2001005046 A1 Cont of US 1999-260218 19990301, US 2001-753735 20010102; US 6323546 B2 Cont of US 1999-260218 19990301, US 2001-753735 20010102; TW 442873 A TW 1999-100499 19990114
FDT US 6323546 B2 Cont of US 6252300
PRAI TW 1999-100499 19990114
AB US2001005046 A UPAB: 20020128
NOVELTY - Direct contact through hole type wafer has devices and contacts on both sides of the wafer. The contacts are coupled with the devices and bumps are formed on the contacts.
DETAILED DESCRIPTION - Direct contact through hole type wafer structure comprises:
(a) a silicon-on-insulator substrate comprising first and second

silicon substrates with a first insulation layer between them. At least one opening is formed in the second silicon substrate which penetrates through the first insulation layer into the first silicon substrate;

(b) at least one device on the first silicon substrate;

(c) a number of contact plugs positioned in the first silicon substrate and exposed by the opening;

(d) a number of dielectric layers and a number of patterned conductive layers which couple with the device and the contact plugs and a number of plugs in the dielectric layers. The dielectric layers and patterned conductive layers are alternately **stacked** on the first silicon substrate. At least one **bonding pad** is formed on the uppermost conductive layer and exposed by an uppermost conductive layer formed on the uppermost conductive layer;

(e) a second insulation layer positioned in the opening. The second insulation layer lies on the surface of the opening and exposes the contact plugs;

(f) a barrier layer which is positioned on the second insulation layer and is coupled with the contact plugs; and

(g) a metal layer which is positioned on the barrier layer.

INDEPENDENT CLAIMS are also included for the following:

(i) a direct contact through hole type wafer structure comprising: a substrate having first and second surfaces; at least one device positioned on the first surface; a first contact positioned over the first surface and coupled with the device; and a second contact positioned over the second surface and coupled with the device; and

(ii) a three-dimensional **stacked**-type package comprising: a substrate on which a number of chips having contacts are attached.. The chips are **stacked** with each other by the contacts and are coupled to the substrate.

USE - The direct contact through hole type wafer structure is used for forming a wafer-level package.

ADVANTAGE - Since both sides of the wafer have contacts, the chips can be easily **stacked** especially three dimensionally. Since the package is a wafer-level package and **stacked** three dimensionally, the volume and height of the package are decreased. Since the chips are coupled with other chips or the printed circuit board by the bumps, the signal transmitting path is reduced which leads to reduced electrical impedance. Problem of signals delaying and decaying is avoided.

Dwg.0/4

L37 ANSWER 5 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-202099 [20] WPIX
DNN N2001-144122 DNC C2001-059969
TI Forming an aluminum contact electrically connected with copper wiring in an integrated circuit comprises forming aluminum **stack** on barrier layer and patterning and etching **stack** and barrier layer.
DC L03 U11
IN COSTRINI, G; GOLDBLATT, R D; HEIDENREICH, J E; MCDEVITT, T L
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 3
PI US 6187680 B1 20010213 (200120)* 10p
KR 2000028654 A 20000525 (200120)
TW 404038 A 20000901 (200120)
ADT US 6187680 B1 US 1998-167834 19981007; KR 2000028654 A KR 1999-38815 19990911; TW 404038 A TW 1999-102628 19990223
PRAI US 1998-167834 19981007
AB US 6187680 B UPAB: 20010615
NOVELTY - Forming an aluminum contact electrically connected with copper

wiring comprises forming, in sequence, a passivating layer, terminal via openings, barrier layer and aluminum **stack** on an integrated circuit semiconductor wafer having an embedded copper wiring; patterning and etching aluminum **stack** and barrier layer; and forming second passivating layer and openings.

DETAILED DESCRIPTION - Forming an aluminum (Al) contact electrically connected with copper (Cu) wiring (22) comprises forming a passivating layer (24) on an integrated circuit (IC) semiconductor wafer (20) having an embedded Cu wiring. Terminal via openings are formed through the passivating layer to expose the Cu wiring. A barrier layer (28) is formed at least over the exposed Cu wiring, on the side walls of the terminal via openings and on regions of the barrier layer near the terminal via openings. An Al **stack** (30) is formed on the barrier layer at least in the terminal via openings and on regions of the barrier layer near the terminal via openings. The Al **stack** and the barrier layer are patterned and etched. A second passivating layer (32) is formed over the patterned Al **stack**. Second openings are provided in the second passivating layer to expose regions of the patterned Al **stack** on top of the Cu wiring.

USE - For forming an aluminum contact electrically connected with copper wiring in an integrated circuit.

ADVANTAGE - The method protects the Cu wiring from environmental exposure or attack by etching chemistries and from the problem of Cu-Al intermixing.

DESCRIPTION OF DRAWING(S) - The figure shows the integrated circuit structure of the invention.

Wafer 20
Cu wiring 22
Passivating layer 24
Barrier layer 28
Al **stack** 30
Second passivating layer 32
Dwg.4b/5

L37 ANSWER 6 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-271087 [23] WPIX
DNN N2000-203060
TI Interface device between testing equipment and integrated circuit, includes contacts each of which includes contact end and casing unit whose central axes are substantially parallel to each other.
DC S01 U11
IN SAWHILL, R A; SHAH, P I
PA (SPIR-N) SPIRE TECHNOLOGIES PTE LTD
CYC 83
PI WO 2000014558 A1 20000316 (200023)* EN 24p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
AU 9891961 A 20000327 (200032)
TW 417229 A 20010101 (200134)
ADT WO 2000014558 A1 WO 1998-SG68 19980909; AU 9891961 A AU 1998-91961 19980909, WO 1998-SG68 19980909; TW 417229 A TW 1998-117735 19981027
FDT AU 9891961 A Based on WO 200014558
PRAI WO 1998-SG68 19980909
AB WO 200014558 A UPAB: 20000516
NOVELTY - Interface device (2) includes a casing (7) and a movable unit

(8) **mounted** on casing for movement with respect to casing. Several elongated contacts (5) are **mounted** on movable unit for movement with the moving unit. Each contact has a contact end adapted to contact a **bond pad** of IC to be tested, and a casing unit (11). Central axis of casing unit and contact end are substantially parallel to each other.

DETAILED DESCRIPTION - The contact comprises a spring shaped portion located between the contact end and casing unit. The central axis of contact end and casing unit are separated by a distance approximately equal to 1.5 times the diameter of the casing unit. The angle of about 45-135 deg. is maintained between two portions of contact.

USE - Interface is connected between testing equipment such as probe and semiconductor integrated circuit to be tested.

ADVANTAGE - As contact end is substantially parallel to the casing unit it is possible to obtain better contact between contact and **bond pad** on chip to be tested. As contact end and spring shaped casing are offset in vertical axis, contact are permitted to be located closer to each other, while minimizing risk of the casing unit contacting each other.

DESCRIPTION OF DRAWING(S) - The figure shows schematic perspective view of interface device.

Interface device 2
Elongated contacts 5
Casing 7
Movable unit 8
Casing unit 11
Dwg.1/9

L37 ANSWER 7 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-125793 [11] WPIX
DNN N2000-094796 DNC C2000-038232
TI Component **stacking** arrangement used for semiconductor dies or chips.
DC L03 U11
IN JENSEN, R J; SPEERSCHNEIDER, C J; SPIELBERGER, R K
PA (HONE) HONEYWELL INC
CYC 1
PI US 6005778 A 19991221 (200011)* 9p
ADT US 6005778 A CIP of US 1995-490635 19950615, US 1996-681784 19960729
PRAI US 1996-681784 19960729; US 1995-490635 19950615
AB US 6005778 A UPAB: 20000301

NOVELTY - The arrangement includes a first die secured to a die **mounting** surface (16). Wire bonds extend from **bonding pads** (26) on the first die to external **bonding pads** (18). A second die is secured to a flat spacer (30). Wire **bonds** extend from **pads** (46) on the second die to the external **bonding pads**.

DETAILED DESCRIPTION - The spacer has an outer tier and a central tier with electrically interconnected conductive surfaces. A conductor electrically connects the conductive surface of the outer tier to a first voltage. The spacer comprises silicon and the conductive surfaces comprise a metal suitable for wire bond connections. The first voltage is located external to the first die. The second die preferably includes:

(1) a dielectric layer secured to the conductive surface;

(2) an electrically conductive layer secured to the dielectric layer; and

(3) an opening extending through the electrically conductive layer and the dielectric layer.

The spacer comprises silicon carbide, aluminum nitride or copper

tungsten.

USE - The component **stacking** arrangement is used for semiconductor dies or chips.

ADVANTAGE - Provides a packaging arrangement which reduces propagation delays, reduces transmission line effects, provides for effective **mounting** and connection of decoupling capacitors and provides more IC function per unit volume of space by increasing the chip packaging density.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the chip **stacking** arrangement.

Die **mounting** surface 16

Bonding pads 18,26

Spacer 30

Dwg.1/10

L37 ANSWER 8 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-065186 [06] WPIX
DNN N2000-051130
TI Structural **mounting** of semiconductor device.
DC U11
IN MORI, F
PA (NIDE) NEC CORP; (MORI-I) MORI F
CYC 3
PI FR 2779867 A1 19991217 (200006)* 29p
JP 11354677 A 19991224 (200011) 9p
JP 3070579 B2 20000731 (200041) 8p
US 2001040791 A1 20011115 (200172)
ADT FR 2779867 A1 FR 1999-7262 19990609; JP 11354677 A JP 1998-161646 19980610; JP 3070579 B2 JP 1998-161646 19980610; US 2001040791 A1 US 1999-328894 19990609
FDT JP 3070579 B2 Previous Publ. JP 11354677
PRAI JP 1998-161646 19980610
AB FR 2779867 A UPAB: 20000203

NOVELTY - The method of **mounting** includes the bonding of the upper surface of semiconductor (30) to a plate (50), the positioning so that the input/output terminals (31) are opposite to plots (11) on a printed substrate (10) with intermediate connecting elements (20), the melting of the connecting elements by heating, and cooling to normal temperature. The coefficient of thermal expansion of the plate is close or equal to that of the substrate, and the bonding of the semiconductor becomes a function of that of the plate.

DETAILED DESCRIPTION - The semiconductor device is an integrated circuit (IC), or a large-scale integration (LSI) implementation. The plate (50) is metallic, made of e.g. copper or brass, and the connecting elements are balls of solder. The adhesive is of epoxy type, and is applied in a layer of thickness 10-20 micrometers. An organic substrate can be used instead of the metallic plate, as well as the printed substrate. In the case of ceramic substrate, the plate is made of aluminum nitride, or ceramic compounds of aluminum or **tungsten**, and a conducting adhesive is used instead of solder. The plate can be in the form of a lid enclosing the semiconductor. The **mounting** can include a heat-dissipating element fastened by screws to the metallic plate.

USE - In fabrication of semiconductor devices, in particular in **mounting** of flip chips.

ADVANTAGE - Improved reliability of semiconductor devices, due to compensation of different rates of thermal expansion.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view of the structural **mounting**.

Substrate 10
Plots 11
Connecting elements 20
Semiconductor 30
Terminals 31
Layer of adhesive 40
Plate 50
Dwg.1/6

L37 ANSWER 9 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-606825 [52] WPIX
DNN N1999-447883 DNC C1999-176891
TI Solder bonding structure for carrier **mounted** semiconductor laser for optical transmission - has aluminum nitride or silicon carbide submount on copper **tungsten** alloy carrier through eutectic solder.
DC L03 U11 U12 V08
PA (HITA) HITACHI LTD
CYC 1
PI JP 11266053 A 19990928 (199952)* 4p
ADT JP 11266053 A JP 1998-66496 19980317
PRAI JP 1998-66496 19980317
AB JP 11266053 A UPAB: 19991210
NOVELTY - A distribution feedback type semiconductor chip (1) having dimension of 0.6 mm multiply 0.4 mm multiply 0.13 mm is **mounted** on 0.9 mm multiply 1.7mm multiply 0.25 mm ceramic AlN or SiC submount (2) through an Au or Sn eutectic solder (3). The linear expansion coefficient of the submount is 3.8 multiply 10-6 deg. C. The melting point of the solder is 280 deg. C.
DETAILED DESCRIPTION - Ceramic AlN or SiC submount (2) loaded with a chip (1) is fixed on a copper-**tungsten** alloy carrier (4) through an Au or Sn eutectic solder (3). The melting point of solder is 280 deg. C. The linear expansion coefficient of the **tungsten** carrier is 4.5 multiply 10-6 deg. C. The different between the expansion coefficient of **tungsten** carrier and ceramic submount is maintained below 1 multiply 10 -6 deg. C.
USE - For carrier **mounted** semiconductor laser for optical transmission.
ADVANTAGE - Favorable laser radiation is obtained by reducing stress caused in **mounting** of carrier submount and chip using solder. Reduces defective incidence rate by using **tungsten** carrier and ceramic submount.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of laser. (1) Semiconductor chip; (2) Ceramic submount; (3) Eutectic solder; (4) Carrier.
Dwg.1/2

L37 ANSWER 10 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-404520 [34] WPIX
DNN N1999-301488
TI Hermetic packaging technology for silicon Schottky die or other two terminal die.
DC U11
IN AUTRY, T; LYNCH, F; TULBURE, D
PA (MICR-N) MICROSEMI CORP
CYC 1
PI US 5923083 A 19990713 (199934)* 6p
ADT US 5923083 A US 1997-810179 19970301
PRAI US 1997-810179 19970301

AB US 5923083 A UPAB: 19990825
NOVELTY - A silicon die (10) is completely enclosed by a ceramic frame (16) **bonded** to **pads** by a sealant. A spacer about 0.005 inches thick is provided in the lower surface of the die is shaped to produce a uniform thickness so that each major surface of the spacer consists of a single plane. A ceramic frame consisting of mullite surrounds the die and the pads which have a thickness of about 0.030 inches.

DETAILED DESCRIPTION - The die has solderable metallization contacts on each of its major surfaces. A pair of metallic pads (12,13) comprising **tungsten** or molybdenum are bonded to the upper surfaces of the die and the spacer, respectively.

USE - Used in military and space systems.

ADVANTAGE - Since solderable metallization which provides direct electrical and thermal connection to the die is obtained, the packaged device is **mounted** in either direction and removes the need for a reverse polarity device. As easily available non-alloys like molybdenum and **tungsten** are used as die pads, the cost of the package is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded view of the package comprising a pressed mullite frame, molybdenum pads, **tungsten** disc alloy, seal rings and the Schottky die.
silicon die 10
metallic pads 12,13
ceramic frame 16
Dwg.2/2

L37 ANSWER 11 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-190734 [16] WPIX
CR 1996-069030 [07]; 1996-354738 [35]; 1996-354740 [35]; 1999-190285 [16]
DNN N1999-139490 DNC C1999-056212
TI Vertical interconnection and **stacking** of segments of silicon using a thermally conductive preform.
DC A21 A35 A60 A85 L03 U11
IN SAUTTER, K M; VINDASIUS, A
PA (CUBI-N) CUBIC MEMORY INC; (CUBI-N) CUBIC MEMORY
CYC 82
PI WO 9910925 A1 19990304 (199916)* EN 57p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
US 5891761 A 19990406 (199921)
AU 9891052 A 19990316 (199930)
EP 1029346 A1 20000823 (200041) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 6124633 A 20000926 (200051)
US 6177296 B1 20010123 (200107)
KR 2001022895 A 20010326 (200161)
JP 2001514449 W 20010911 (200167) 57p
ADT WO 9910925 A1 WO 1998-US16901 19980814; US 5891761 A CIP of US 1994-265081 19940623, US 1997-918502 19970822; AU 9891052 A AU 1998-91052 19980814; EP 1029346 A1 EP 1998-943211 19980814, WO 1998-US16901 19980814; US 6124633 A CIP of US 1994-265081 19940623, US 1997-918501 19970822; US 6177296 B1 CIP of US 1994-265081 19940623, Cont of US 1997-918502 19970822, US 1999-273941 19990322; KR 2001022895 A KR 2000-701499 20000214; JP 2001514449 W WO 1998-US16901 19980814, JP 2000-508139 19980814
FDT US 5891761 A CIP of US 5675180; AU 9891052 A Based on WO 9910925; EP 1029346 A1 Based on WO 9910925; US 6124633 A CIP of US 5675180; US 6177296 B1 CIP of US 5675180, Cont of US 5891761; JP 2001514449 W Based on WO 9910925
PRAI US 1997-918502 19970822; US 1997-918501 19970822; US 1994-265081 19940623; US 1999-273941 19990322
AB WO 9910925 A UPAB: 20020105
NOVELTY - Vertically adjacent segments in the **stack** are electrically interconnected by applying electrically conductive epoxy filaments or lines to one or more sides of the **stack**. A thermally conductive epoxy preformed sheet is provided so that the **stack** of segments are epoxied together.

DETAILED DESCRIPTION - The **stack** of electrical circuitry comprises a **stack** of segments vertically placed on top of one another, each of the segments including a plurality of edges, a plurality of die having circuitry therein, and electrically conductive contact points. The plurality of die on a segment are interconnected on the segment using one or more layers of metal interconnects which extend to all 4 sides of the segment to provide edge **bonding pads** for external electrical connection points. The die are interconnected and each segment is cut from the backside of the wafer using a bevel cut to provide 4 inwardly sloping edge walls on each of the segments.

After the segments are cut from the wafer, the segments are placed on top of one another to form a **stack**. Vertically adjacent segments in the **stack** are electrically interconnected by applying

electrically conductive epoxy filaments or lines to one or more sides of the **stack**, the inwardly sloping edge walls of each of the segments in the **stack** providing a recess which allows the epoxy to access the edge **bonding pads** and lateral circuits on each of the segments once the segments are **stacked**.

A thermally conductive epoxy preformed sheet is provided so that the **stack** of segments are epoxied together. The thermally conductive epoxy preform includes a plurality of glass spheres randomly distributed within the preform to maintain a distance between the **stack** of segments.

USE - A method and apparatus for **stacking** and interconnecting segments of silicon using a vertical interconnect process, useful, e.g. in a Personal Computer Memory Card International Association (PCMCIA) card.

ADVANTAGE - The epoxy preform provides increased package strength and improved thermal characteristics in removing heat from between the layers of the high density integrated circuit package.

DESCRIPTION OF DRAWING(S) - The diagram shows a method for providing a vertical electrical path between segments in a **stack**.

Segments 36

External **bond pads** 42

beveled edge walls 102

Stack 112

Silvered filled conductive epoxy traces 130

Dwg.10B/17

L37 ANSWER 12 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-579172 [49] WPIX
DNN N1998-451913
TI Semiconductor device for computer - has metal layer formed in protruding manner on titanium, **tungsten** or chrome layer, over which bump electrode is provided.
DC U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 10261642 A 19980929 (199849)* 12p
ADT JP 10261642 A JP 1997-64289 19970318
PRAI JP 1997-64289 19970318
AB JP 10261642 A UPAB: 19981210

The device has a semiconductor chip (1) which is provided with a **bonding pad** (5). A first oxygen content metal layer (3) is formed at the peripheral side of the **bonding pad**.

The metal layer is formed using titanium, **tungsten** or chrome. A second metal layer (4) is formed in protruding manner, on the first metal layer. A bump electrode (2) is formed on the second metal layer.

ADVANTAGE - Enables flip-chip **mounting** with low resistance value. Facilitates **mounting** with high density.

Dwg.1/28

L37 ANSWER 13 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-446104 [38] WPIX
CR 2000-104910 [08]
DNN N1998-347727 DNC C1998-135269
TI Chip module fabrication method for e.g. multi chip module - by providing substrate with pattern of microbumps formed on insulating film which contact locations on die, and **mounting** die to substrate using adhesive layer.
DC A85 G03 L03 U11 U14

IN AKRAM, S; FARNWORTH, W M; WOOD, A G
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5789278 A 19980804 (199838)* 13p
ADT US 5789278 A US 1996-688368 19960730
PRAI US 1996-688368 19960730
AB US 5789278 A UPAB: 20000218
The method for fabricating a chip module involves (a) providing a semiconductor die with several contact locations, (b) providing a substrate which includes a pattern of contacts formed on it, the contacts include microbumps formed on an insulating film attached to the substrate, the contacts provide electrical connections with the contact locations and (c) **mounting** a semiconductor die to the substrate using a conductive adhesive layer to electrically connect the contacts on the substrate to the contact locations on the die.

There is also a conductor on the insulating film in electrical communication with each microbump. The insulating film comprises a multi layered tape. A cap layer is also formed on each microbump. The cap layer includes a non-oxidising material e.g. gold, palladium, **tungsten**, platinum or alloys of these materials. The insulating film comprises a multi layered tape with conductors on it. An anisotropic adhesive layer comprising a z-axis epoxy, is formed between the substrate and the insulating film. An underfill layer is formed between the insulating film and the substrate.

USE - Also for memory modules.

ADVANTAGE - Allows low resistivity contacts to be made between die and substrate with minimal damage to **bond pads** of die.

Dwg.2A/7

L37 ANSWER 14 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-101319 [09] WPIX
CR 1995-200548 [26]; 1996-260007 [26]; 1996-260008 [26]; 1996-260071 [26]; 1996-268811 [27]; 1996-278048 [28]; 1997-021018 [02]; 1997-021019 [02]; 1997-021020 [02]; 1997-021021 [02]; 1997-021477 [02]; 1997-034628 [03]; 1997-272356 [24]; 1998-009059 [01]; 1998-009060 [01]; 1998-009062 [01]; 1998-018661 [02]; 1998-610653 [51]; 1998-610654 [51]; 1999-010068 [01]; 1999-096024 [08]; 1999-254404 [21]; 1999-357183 [30]; 2000-170958 [09]; 2000-282503 [23]; 2000-374484 [29]; 2000-412484 [35]; 2000-442216 [36]; 2000-490298 [41]; 2001-520831 [57]; 2002-096877 [74]
DNN N1998-081166
TI Electronic assembly with elongate interconnection elements - has free ends for making connection with terminals of micro-electronic components, and floating lateral support with holes through which free ends of connection elements extend.
DC S01 U11
IN ELDRIDGE, B N; KHANDROS, I Y; MATHIEU, G L; TAYLOR, S A
PA (FORM-N) FORMFACTOR INC
CYC 75
PI WO 9801906 A1 19980115 (199809)* EN 28p
RW: AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN
AU 9736034 A 19980202 (199826)
ADT WO 9801906 A1 WO 1997-US12541 19970703; AU 9736034 A AU 1997-36034 19970703
FDT AU 9736034 A Based on WO 9801906
PRAI WO 1997-US8606 19970515; US 1996-21667P 19960705; US 1996-24405P

19960822; US 1997-788740 19970124; US 1997-779020 19970210; US 1997-819464 19970317; US 1997-824988 19970327

AB WO 9801906 A UPAB: 20020226
The assembly comprises electronic component having a surface, number of elongate connection elements extending from surface of component, with each interconnection element **mounted** by base end to the surface of the electronic component, and a planar element having a number of through holes, each of which corresponds to one elongate interconnection element.

The electronic component may be a space transformer component of probe card assembly, and the elongate interconnection elements may be spring contacts elements, or **tungsten** needles, or composite interconnection elements.

ADVANTAGE - Effect pressure connections to terminals of electronic components, such as semiconductor devices resident on semiconductor wafer, protected from adverse lateral forces.
Dwg.2A/3

L37 ANSWER 15 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1996-326814 [33] WPIX
DNN N1996-275324 DNC C1996-103649
TI Semiconductor device for **mounting** semiconductor chip on substrate - having aluminium (alloy) electrodes, and electrode of low fusing pt. metal such as tin , tin -lead alloy or lead, to which bump of semiconductor chip is connected.
DC L03 U11 V04
PA (YAWA) NIPPON STEEL CORP
CYC 1
PI JP 08148496 A 19960607 (199633)* 5p
ADT JP 08148496 A JP 1994-309967 19941118
PRAI JP 1994-309967 19941118
AB JP 08148496 A UPAB: 19960823
The semiconductor device consists of a semiconductor chip (10) in which multiple Al electrodes (11) are provided at desired portion. The Al electrode is made of either Al alloy, titanium, nickel, titanium-**tungsten** alloy, chromium or copper. The film thickness of the electrode is formed to be more than 0.001 microns.

A bump (14) comprising a snow white metal or platinum alloy is connected to the electrode. An electrode (16) which is made up of low fusing point metal such as tin or tin-lead alloy is provided on the substrate (15). A substrate electrode is then connected with bump.

ADVANTAGE - The device improves reliability in **mounting** semiconductor, and prevents adhesion of solder of bump effectively.
Dwg.2/2

L37 ANSWER 16 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1996-084428 [09] WPIX
DNN N1996-070794 DNC C1996-027314
TI Ceramic substrate with bump for **mounting** chip carrier in external mother board - has thick film electric conductor made from **tungsten** and/or molybdenum and iridium which connect internal wiring layer and copper ball, gives reliable junction and withstands **mounting** conditions.
DC L03 M26 U11 U14 V04
PA (SUMI-N) SUMITOMO KINZOKU CERAMICS KK
CYC 1
PI JP 07335782 A 19951222 (199609)* 5p
ADT JP 07335782 A JP 1994-130540 19940613
PRAI JP 1994-130540 19940613

AB JP 07335782 A UPAB: 19960305
Ceramic substrate (1) has number of wiring layers (2) in and on the surface. A thick film electric conductor (3) made from W and/or Mo (40-90 wt. %) and Ir (60-10 wt. %) connects the wiring layer and a copper ball (4).
USE/ADVANTAGE - In **mounting** ceramic substrate, ceramic chip connector which connects semiconductors e.g. IC. Offers reliable junction. Withstands influence of **mounting** condition.
Dwg.1/3

L37 ANSWER 17 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-306117 [40] WPIX
DNN N1995-232263
TI Hybrid integrated circuit board for **mounting** of e.g. semiconductor element - has circuit pattern made of refractory metal embedded within and protruding from ceramic substrate and adhered by layer of nickel.
DC U14 V04
PA (KYOC) KYOCERA CORP; (TOYT) TOYOTA JIDOSHA KK
CYC 1
PI JP 07202356 A 19950804 (199540)* 5p
ADT JP 07202356 A JP 1993-335233 19931228
PRAI JP 1993-335233 19931228
AB JP 07202356 A UPAB: 19951019
The device, constituting a multilayer circuit board, has circuit pattern (2) made of refractory metal (e.g. **tungsten**, molybdenum, manganese) imbedded within and protruding from a ceramic substrate (1). The conducting circuit pattern (4) on the surface is of copper. The pattern interconnection (4) and the **bonding pad** (2a) is layered by contact metal layer (3). The pad (2a) is then layered by covering layer (5) while the interconnection with copper.
The covering layer, made of nickel with a grade of 600 on the Vickers Hardness scale, is provided to prevent deformation by heat of bonding surface during thermocompression (or by ultrasonic) bonding of the wire from the active component to this pad.
ADVANTAGE - More reliable multilayer circuit implementation through better bonding of wire to the pad of this substrate.
Dwg.1/2

L37 ANSWER 18 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1993-136747 [17] WPIX
DNN N1993-104315 DNC C1993-060877
TI Formation of earth electrode of electric circuit **mounting** case - by radiating arc generated from torch and **tungsten** electrode to melt aluminium case and remove gas before arc welding NoAbstract.
DC M23 U11
PA (AICI) AICHI SEIKO KK; (NPDE) NIPPONDENSO CO LTD
CYC 1
PI JP 04242961 A 19920831 (199317)* 5p
ADT JP 04242961 A JP 1991-739 19910108
PRAI JP 1991-739 19910108

L37 ANSWER 19 OF 29 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1987-037371 [05] WPIX
DNN N1987-028321
TI Laminated structure to connect substrates - uses several layers of solder bumps provided with layered metals of different solder wettability.
DC U11 U14 V04
IN EGAWA, Y; MATSUI, N; OSAKI, T; SASAKI, S

PA (NITE) NIPPON TELEGRAPH & TELEPHONE CORP; (OSAK-I) OSAKI T
CYC 6
PI WO 8700686 A 19870129 (198705)* JA 45p
RW: DE FR GB NL
W: US
JP 62018049 A 19870127 (198709)
EP 229850 A 19870729 (198730) EN
R: DE FR GB NL
JP 62293730 A 19871221 (198805)
US 4783722 A 19881108 (198847) 22p
US 4897918 A 19900206 (199012) 22p
EP 229850 B1 19920610 (199224) EN 37p
R: DE FR GB NL
DE 3685647 G 19920716 (199230)
ADT WO 8700686 A WO 1986- 19860716; EP 229850 B1 EP 1986-904381 19860716, WO 1986-JP364 19860716; DE 3685647 G DE 1986-3685647 19860716, EP 1986-904381 19860716, WO 1986-JP364 19860716
FDT EP 229850 B1 Based on WO 8700686; DE 3685647 G Based on EP 229850, Based on WO 8700686
PRAI JP 1985-156621 19850716; JP 1986-137961 19860613
AB WO 8700686 A UPAB: 19930922
Terminals (b,d) on an IC chip (a) and a printed circuit board (c) are connected by using a laminated structure comprising solder bumpers (e), a ceramic sheet (j) and multi-layered metal elements (l,k,l'). The surfaces of the metal elements are made of solder-wettable material, such as copper, and the centres (m) are made of solder-non wettable material, such as **tungsten** or molybdenum, so that both surfaces can be soldered separately.

Each plate element is manufactured by punching through holes on a ceramic green sheet and then filling the holes with copper, **tungsten**, and copper paste, successively. This is then connected with another by using solder bumpers (e) to form the laminated structure, with which the chip and the printed circuit board are finally connected.

ADVANTAGE - Large height of solder bumpers improves lifetime of connection.
1/4

L37 ANSWER 20 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 2000-164928 JAPIO
TI SEMICONDUCTOR LIGHT EMITTING DEVICE AND ITS MANUFACTURE
IN OKAZAKI HARUHIKO; NOZAKI CHIHARU; FURUKAWA CHISATO
PA TOSHIBA ELECTRONIC ENGINEERING CORP
TOSHIBA CORP
PI JP 2000164928 A 20000616 Heisei
AI JP1998-334574 (JP10334574 Heisei) 19981125
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To improve ohmic characteristic by forming, in a p-side electrode, a contact layer which includes silver, in contact with a layer made of p-type nitride semiconductor and forming a layer made of **tungsten** on the contact layer.
SOLUTION: A p-side electrode is constituted of a light transmitting electrode and a **bonding pad** section. More specifically, a block layer 13 comprising at least SiO2 is selectively formed on a p-type GaN contact layer 9 and then a light transmitting electrode **stacked** with a first metal layer 10, second metal layer 11, and **tungsten** layer 12 is formed on the rest of the surface, As the first metal layer 10, silver is preferably used. As the second metal layer 11, gold is preferably used. By using either silver or a mixture of silver and gold for contact metal to be brought into contact

with the p-type contact layer 9, an ohmic contact with the p-type contact layer 9 can be improved.
COPYRIGHT: (C)2000,JPO

L37 ANSWER 21 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 2000-091341 JAPIO
TI PROCESSING FOR COPPER-**BONDED PAD**
IN STEPHEN W RUSSELL; LU JOING-PING
PA TEXAS INSTR INC <TI>
PI JP 2000091341 A 20000331 Heisei
AI JP1999-260357 (JP11260357 Heisei) 19990914
PRAI US 1998-100335 19980915
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To improve bonding which uses a copper pad.
SOLUTION: Copper wirings 40 and 50, using an integrated circuit, have copper-**bonded pads** 20 covered by inert layers so that they prevent the undesired reaction of bonded metal and copper. The inert layers can be the **stack** layers of the alloy of copper and titanium or CuTix/TiN. Nitride such as **tungsten** nitride, tantalum nitride, silicon titanium nitride and silicon tantalum nitride can similarly be used.
COPYRIGHT: (C)2000,JPO

L37 ANSWER 22 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1995-202356 JAPIO
TI CIRCUIT BOARD
IN YAMAMOTO KEIJI; HOSOI YOSHIHIRO
PA TOYOTA MOTOR CORP, JP (CO 000320)
KYOCERA CORP, JP (CO 358923)
PI JP 07202356 A 19950804 Heisei
AI JP1993-335233 (JP05335233 Heisei) 19931228
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 8
AB PURPOSE: To provide a circuit board which can join a bonding wire and a circuit conductor firmly and quickly when directly **mounting** an active element such as a semiconductor element on the circuit board without any package.
CONSTITUTION: A wiring conductor 2 consisting of high melt-point metal made of **tungsten**, molybdenum, manganese, etc., is formed inside and on the surface of an insulation board 1 such as ceramic and further a circuit conductor 4 consisting of copper is deposited so that the surface of the exposed wiring conductor 2 is covered. A **bonding pad** 2a is formed at a part which is exposed on the outer surface of the insulation board 1, a covering layer 5 which mainly consists of nickel with a Vickers hardness of 600 or larger is deposited on the surface of the **bonding pad** 2a, and a bonding wire which is connected from the area on the covering layer 5 to each electrode of the semiconductor element A.

L37 ANSWER 23 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1991-149862 JAPIO
TI SEMICONDUCTOR DEVICE
IN SASAKA MASAAKI
PA FUJITSU LTD, JP (CO 000522)
KYUSHU FUJITSU ELECTRON:KK, JP (CO)
PI JP 03149862 A 19910626 Heisei
AI JP1989-289114 (JP01289114 Heisei) 19891107
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1114, Vol. 15, No. 375, P. 118 (19910920)

AB PURPOSE: To obtain a highly moisture-resistant device not damaged by water absorbed by mold resin even after heating such as solder packaging by coating the rear of a die pad with a silicon semiconductor or a metallic film.
CONSTITUTION: The present invention comprises a die pad 2, a silicon IC chip 6 **mounted** on the surface thereof, **bonding pads** 7 formed on the surface of the chip 6, leads 3 connected with bonding wires 8, a silicon semiconductor or metallic film 5 to coat the rear of the die pad 2, and mold resin 9 to mold the IC chip 6, the die pad 2, the silicon semiconductor or metallic film 5, the bonding wires 8, and part of the leads 3. For example, the silicon semiconductor or metallic film 5 is made of one or more of polycrystalline silicon, amorphous silicon, **tungsten** silicide, molybdenum silicide, and titanium silicide.

L37 ANSWER 24 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1991-030454 JAPIO
TI CERAMIC LAMINATED PACKAGE
IN TAKAMICHI HIROSHI; SUMIDA YUKITSUGU
PA NARUMI CHINA CORP, JP (CO 352544)
PI JP 03030454 A 19910208 Heisei
AI JP1989-166189 (JP01166189 Heisei) 19890628
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1059, Vol. 15, No. 159, P. 61 (19910422)
AB PURPOSE: To relax a load imposed on an uppermost layer so as to prevent cracks from starting from the root of a step by a simple structure by a method wherein a reinforcing metallized layer of high melting point metal is provided on the root of the step between the uppermost layer and the second layer.
CONSTITUTION: In a ceramic laminated package on which semiconductor elements are **mounted**, a reinforcing metallized layer 13 of high melting point metal is provided on the root 11 of a step between an uppermost part 4 and a second part 3 of a ceramic laminated board 5. For instance, the ceramic green sheets of layers 1-5 are cut into required sizes respectively, and a positioning guide hole, a semiconductor element **mounting** part, a through-hole, and the like are punched in the layers 1-5 respectively. Furthermore, a die **pad** 6, a **bonding pad** 8, an inner wiring layer 9, the conduction of the through- hole, and an reinforcing metallized layer 13 are formed through printing with **tungsten** paste. Then, the layers 1-5 are hot-bonded by press at a temperature of 100-120.degree.C to form a laminated piece, which is subjected to a reducing burning process at a temperature of 1500-1600.degree.C, then Ni, Au, or the like is plated as required, input-output pins 10 are brazed, and thus a laminated package is formed.

L37 ANSWER 25 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1990-090655 JAPIO
TI PACKAGE FOR SEMICONDUCTOR USE
IN SUZUKI KATSUHIKO
PA NEC CORP, JP (CO 000423)
PI JP 02090655 A 19900330 Heisei
AI JP1988-245033 (JP63245033 Heisei) 19880928
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 942, Vol. 14, No. 282, P. 138 (19900619)
AB PURPOSE: To reduce a continuity resistance and to adapt to the high-speed operation of a semiconductor device as well by a method wherein, in each layer of lower-stage, middle-stage and upper-stage metallized layers, which are printed on an insulating substrate and an insulating layer, the

metallized layer is directly extended from a **bonding pad** to a lead connecting part and is led out directly to the exterior without the mediation of a through hole.
CONSTITUTION: A lower-stage metallized layer 3 consisting of **tungsten** or the like, which is arranged on the peripheral edge of an opening part of a ceramic substrate 1 having the opening part at its central part and is arranged toward the outer periphery of the substrate 1, is provied. Then, an insulating layer 12a is provided on the surface, from which the surface in the vicinity of the opening part and the vicinity of the outer periphery of the substrate 1 is excepted, of the layer 3 and a middle-stage metallized layer 11 is provided on the layer 12a in a way identical with a way of providing the layer 3. In the same way, an insulating layer 12b and an upper-stage metallized layer 4 are provided on the surface including the surface of the layer 11 and an insulating layer 12c is provided on the surface including the surface of the layer 4. A heat sink 10 with an element placing part 2 provided thereon is inserted and fixed in the opening part, a semiconductor chip 14 is **mounted** on the placing part 2 and each metallized layer at each **bonding pad** part and electrodes of the chip 14 are electrically connected to each other.

L37 ANSWER 26 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1989-321664 JAPIO
TI RESIN SEALED SEMICONDUCTOR DEVICE
IN NAKAMURA TAKU
PA NEC CORP, JP (CO 000423)
PI JP 01321664 A 19891227 Heisei
AI JP1988-156101 (JP63156101 Heisei) 19880623
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 901, Vol. 14, No. 13, P. 118 (19900312)
AB PURPOSE: To improve moisture resistance of a semiconductor device by providing a metal film which coats the surfaces of metal parts including **bonding pads** and wires.
CONSTITUTION: Al pads 2 and Au wires 4 which are located on the surface of a semiconductor chip 1 and internal and external leads 6 and 5 are electrically connected one another and then, side faces of an island 8 and the semiconductor chip have metal faces through an Ag paste 9. This device allows a W selective CVD process which uses reductive reaction by use of an S1H4 gas of WF6 to coat the metal faces out of interfaces between a resin part 11 and respective parts with a W-Si (**tungsten** silicide) film 10 at about 0.5-1.mu.m. After coating the metallic faces with the W-S1 film 10, the faces are sealed with an epoxy resin in the same way as the conventional one and then, the molding processing of an external lead 5 is performed. Conventional, moisture enters through interfaces between the resin part 11 and the internal lead 6 and between the resin part 11 and the Au wires 4, and corrodes the Al pads 2. On the contrary, by the above structure, the paths through which moisture enters can be sealed. In this way, especially after **mounting** of this metal film on a printed board, the moisture resistance of a semiconductor device can be improved.

L37 ANSWER 27 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1988-292693 JAPIO
TI MULTILAYERED CERAMIC WIRING SUBSTRATE CHARACTERIZED BY HIGH HEAT CONDUCTIVITY
IN HAMAGUCHI HIROYUKI; SHIMADA YUZO
PA NEC CORP, JP (CO 000423)
PI JP 63292693 A 19881129 Showa
AI JP1987-126898 (JP62126898 Showa) 19870526

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 733, Vol. 13, No. 123, P. 116 (19890327)

AB PURPOSE: To make it possible to form a high density circuit having conductors including resistors, signal lines, power source layers and the like and to improve heat dissipation property, by providing a resistor layer, whose main component is tantalum nitride, in a ceramic layer constituted with a polycrystalline body, whose main component is aluminum nitride.
CONSTITUTION: An insulating ceramic layer 1 constituted with a polycrystalline body of aluminum nitride as a main component. A resistor 2 is formed with tantalum nitride as a main component. Conductor layers 3 for signal lines, power sources and the like are formed with **tungsten** as a main component. The layers are electrically connected through via holes, which are formed in the insulating ceramic layer. Die **pads** 5 and **bonding pads** 6 are formed on a multilayered ceramic board formed in this way so that LSI chips can be **mounted**. I/O pads 7 are formed on the rear surface of the substrate. Heat that is yielded from the LSIs, which are **mounted** on the substrate, is diffused in the ceramic substrate through the die pads 5.

L37 ANSWER 28 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1985-120541 JAPIO
TI SEMICONDUCTOR DEVICE
IN OZAKI HIROSHI; OKINAGA TAKAYUKI; OTSUKA KANJI
PA HITACHI MICRO COMPUT ENG LTD, JP (CO 470864)
HITACHI LTD, JP (CO 000510)
PI JP 60120541 A 19850628 Showa
AI JP1983-226881 (JP58226881 Showa) 19831202
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 355, Vol. 9, No. 2771, P. 70 (19851106)

AB PURPOSE: To prevent the reliability of a semiconductor device from decreasing due to static electricity by coating a metallized layer on the surface of a ceramic cap in the state electrically connected with a ground terminal.
CONSTITUTION: A pellet 6 is **mounted** with gold-silicon alloy 7 at the center of a cavity 5 of a package substrate 4 buried with metallized layers 3 formed continuously at bothends with external terminal 1 and internal leads 2, the **bonding pad** 8 of the pellet 6 and the leads 2 are then bonded by wirings 9 to be electrically connected, and hermetically sealed by a ceramic cap 11 with low melting point glass 10 as a bonding material. A semiconductor device is formed by **mounting** a cap 11 made of ceramic material of slightly smaller square shape than the substrate 4 and having a projection 12 of the shape projected to the position that coincides with the side of the substrate at the center of one side, on the package substrate 3 of planely square shape, and a metallized layer 13 coated by printing with **tungsten** on the surface of the cap is electrically conducted with the terminal 1 of a ground terminal with metal 14 such as solder.

L37 ANSWER 29 OF 29 JAPIO COPYRIGHT 2002 JPO
AN 1983-197863 JAPIO
TI SEMICONDUCTOR DEVICE
IN MIYAMOTO TAKASHI
PA NEC CORP, JP (CO 000423)
PI JP 58197863 A 19831117 Showa
AI JP1982-80936 (JP57080936 Showa) 19820514
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 228, Vol. 8, No. 391, P. 105 (19840221)

AB PURPOSE: To enhance the general-purpose property of a ceramic substrate whereon semiconductor elements are **mounted** and thus enable the **mount** of many kinds of semiconductor elements with a kind of ceramic substrate by a method wherein the bxtended part of metallic wirings conducted to the back surface or electrode of a semiconductor element is provided close to a metallic terminal.
CONSTITUTION: A metallic layer 10 called an island is provided at the bottom of cavity 2 provided on the ceramic substrate 1, and the semiconductor element 3 is fixed thereon. The island is generally formed by plating Ni and further Au, after screen printing of the ink wherein particles of **tungsten** W or molybdenum Mo are diffused before calcination of the ceramic substrate and calcinating it. Next, the electrodes 11 of the semiconductor element 3 and **bonding pads** 4 are connected by metallic fine wires 5 with Au or Al as the main consistuent. The extended part 12 projects out from the island 10, which is connected to the pad 14 on the surface of the ceramic substrate through a through hole 13. On the other hand, the metallic terminal 15 extend from a metallic ring in access to the pad 14.

L22 ANSWER 1 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2002-132680 [18] WPIX
DNN N2002-100089
TI Chip size **stack** package has metal trace embedded in through hole exposing **bonding pads** of upper and lower semiconductor chips, for connecting **bonding pads** to external terminal.
DC U11 U14
IN PARK, S U
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 2
PI JP 2001035999 A 20010209 (200218)* 9p
KR 2001004042 A 20010115 (200218)
ADT JP 2001035999 A JP 2000-195156 20000628; KR 2001004042 A KR 1999-24627 19990628
PRAI KR 1999-24627 19990628
AB JP2001035999 A UPAB: 20020319
NOVELTY - An **insulating layer** (20) is formed on the **bonding pad** bearing surfaces of each semiconductor chips (40,41) arranged oppositely. The **bonding pads** (11) are exposed by a through hole formed in **insulating layer**. A **metal** trace (30) is embedded in through hole for connecting exposed **bonding pads** to external terminal **via** metal **wire** (80). Both sides of the semiconductor chips are molded by a sealing agent (100).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of chip size **stack** package.
USE - Chip size **stack** package includes DRAM.
ADVANTAGE - Since metal trace connects the **bonding pads** electrically, to external terminal **via wires**, the electric signal transmission path is shortened and the mutual signal interference is minimized. Since sealing agent is coated to sides of semiconductor chips, the defective semiconductor chip is discardable easily and penetration of external moisture content is prevented.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of chip size **stack** package.
Bonding pads 11
Insulating layer 20
Metal trace 30
Semiconductor chips 40,41
Metal wire 80
Sealing agent 100
Dwg.7/26

L22 ANSWER 2 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-655815 [75] WPIX
TI Wafer level package.
DC U11
IN BAEK, H G; LEE, N S
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2001061792 A 20010707 (200175)* 1p
ADT KR 2001061792 A KR 1999-64334 19991229
PRAI KR 1999-64334 19991229
AB KR2001061792 A UPAB: 20011220
NOVELTY - A wafer level package is provided to strengthen an adhesion of a solder ball by using an interconnection medium, in which a support

structure is reinforced, instead of a metal pattern.

DETAILED DESCRIPTION - A **bond pad** is arranged on a surface of a wafer(10), and a pattern film(20) is adhered on the surface of the wafer(10). The pattern film(20) has lower and upper **insulation layers** formed on lower and upper surfaces of a **metal layer**(21) so as to be opposed to each other. An adhesive is placed on a lower surface of the lower **insulation layer**. An etch groove is formed by etching the pattern film(20), and a **bond pad**(11) is exposed through the etch groove. A stepped surface is formed on both sidewalls of the etch groove. The **metal layer**(21) and the **bond pad**(11) are electrically connected **through** a metal **wire**(30). A solder ball(40) is **mounted** at a ball land.

Dwg.1/10

L22 ANSWER 3 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-579990 [65] WPIX
CR 2001-158865 [16]
DNN N2001-431799 DNC C2001-172069
TI Integrated circuit production on substrates, involves depositing dielectric layer on wiring layer, patterning, etching dielectric layer to form grid structures, depositing and patterning **metal** barrier **layer**.
DC A85 L03 U11
IN CHEN, S
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 2001016415 A1 20010823 (200165)* 11p
ADT US 2001016415 A1 Div ex US 1999-442497 19991118, US 2001-755282 20010108
FDT US 2001016415 A1 Div ex US 6191023
PRAI US 1999-442497 19991118; US 2001-755282 20010108
AB US2001016415 A UPAB: 20011108

NOVELTY - A **metal** wiring **layer** is embedded in an **insulating layer** which is provided on a substrate. A passivating dielectric layer is deposited on the **metal** wiring **layer**. The IMD is patterned and etched to form grid structures (6). A blanket of **metal** barrier **layer** is deposited. The **metal** barrier **layer** is patterned on the grid structures. A **metal layer** is deposited and patterned on the grid structures to form metal pad contact structures.

DETAILED DESCRIPTION - A substrate (1) having a layer of dielectric, inter-level dielectric (ILD), or an interconnect layer, or device contact region to P-N junctions, is provided. A first level of metal wiring (3) is embedded in a first **layer** of **insulator** (2). A blanket of passivating dielectric layer (IMD) is deposited on the first level **metal** wiring **layer**. The IMD is patterned and etched to form special interlocking grid structures with open contact regions to underlying first level metal wiring. A blanket of **metal** barrier **layer** (10) is deposited. The **metal** barrier **layer** is patterned on grid structures. A blanket of **metal layer** is deposited and patterned on grid structures to form metal pad contact structures. The process is repeated to construct multilevel pad structures by robust method to form metal pad contact structures for chips, integrated circuits and other applications.

An INDEPENDENT CLAIM is also included for **bond pad** structure which comprises a passivating layer and a barrier layer formed orderly on several conductive **bond pads** on a semiconductor substrate. The passivating layer has multiple openings to each **bond pads**. An upper surface of conductive pads

provide improved adhesion for subsequently formed bonds.
USE - For fabricating integrated circuits and other devices on substrates to form semiconductor integrated circuit devices.
ADVANTAGE - The robust unique metal pad interlocking structures with good adhesion properties, low thermal stress and good conductivity is formed easily and inexpensively in a short period of time by the new and improved method. The interlocking structure form islands of interlocking grid structures (an array in three dimensions) to enhance adhesion among the various **layer** of the **metal stack** pad structure for improved wire bond strength. The interlocking pad structure provides robust pad metal **stack** structures of high reliability. The unique contact pad structure provides thermal stress relief, improved wire bond adhesion to the aluminum pad and prevents peeling during wire bond adhesion tests.
DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of the deposition, patterning and defining of a thin barrier **metal layer** e.g. tantalum nitride on interlocking pad structures.
Substrate 1
Insulator 2
Metal wiring 3
Grid structures 6
Metal barrier **layer** 10
Dwg.2/4

L22 ANSWER 4 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-404446 [35] WPIX
CR 1999-239233 [20]
DNN N1998-315432 DNC C1998-122133
TI BGA package electronic component manufacturing method - involves forming solder bumps on one copper pads formed on surface of substrate.
DC L03 U11
IN HAJI, H; SAKEMI, S
PA (MATU) MATSUSHITA DENKI SANGYO KK; (MATU) MATSUSHITA ELECTRIC IND CO LTD
CYC 3
PI JP 10163241 A 19980619 (199835)* 5p
US 5909633 A 19990601 (199929)
KR 98042929 A 19980817 (199938)
KR 272399 B 20001115 (200170)
ADT JP 10163241 A JP 1996-319105 19961129; US 5909633 A US 1997-979694 19971126; KR 98042929 A KR 1997-64578 19971129; KR 272399 B KR 1997-64578 19971129
FDT KR 272399 B Previous Publ. KR 98042929
PRAI JP 1996-319105 19961129; JP 1997-222196 19970819
AB JP 10163241 A UPAB: 20011129
The method involves forming a pair of copper pads (14,16) on either surfaces of a substrate (11), respectively. A barrier **metallic layer** containing a nickel film is formed on the copper pads. A gold film is formed on the barrier **metallic layer**. A chip (12) is **mounted** on the substrate through a heat cured adhesive agent. A nickel **oxide film** formed on the surface of the gold films is removed by plasma etching.
The copper pads are connected electrically to the chip **through** a **wire** (15). A resin mold seals the chip and the wire on the substrate. A set of solder bamps (17) are formed on one of the copper pads.
ADVANTAGE - Enables satisfactory electrical **bonding** of copper **pads**. Offers satisfactory formation of solder bumps. Provides cheap and reliable electronic component.
Dwg.1/9

L22 ANSWER 5 OF 7 JAPIO COPYRIGHT 2002 JPO
AN 1997-064088 JAPIO
TI SEMICONDUCTOR PHOTODETECTOR AND METHOD FOR **MOUNTING** IT
IN FURUKAWA RYOZO; MINEO NAOYUKI
PA OKI ELECTRIC IND CO LTD, JP (CO 000029)
PI JP 09064088 A 19970307 Heisei
AI JP1995-209825 (JP07209825 Heisei) 19950818
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 3
AB PURPOSE: TO BE SOLVED:To provide a semiconductor photodetector which has an improved frequency response characteristic by suppressing floating capacity increase due to a light shielding **metal film**.
CONSTITUTION: type diffusion area 20 is provided on a part of an window layer 16, and on the window layer 16 around the diffusion layer 20, a shielding film laminate 26, which has a light shielding **metal film** as a middle **layer** in an **insulating film**, is provided. A capacitor is formed between the light shielding **metal film** and the window **layer** 16. A **metal bonding pad** electrode 36, which is electrically connected with the light shielding **metal film** and exposes from the surface of the **insulating film** by penetrating the **insulating film** part on the light shielding **metal film**, is also provided. The potential of the light shielding **metal film** can be dropped to the ground by using bonding **wire through** the metal **bonding pad**.

L22 ANSWER 6 OF 7 JAPIO COPYRIGHT 2002 JPO
AN 1994-314861 JAPIO
TI SUBSTRATE FOR **MOUNTING** ELECTRONIC COMPONENT
IN NOMA HIROSHI
PA IBIDEN CO LTD, JP (CO 000015)
PI JP 06314861 A 19941108 Heisei
AI JP1993-102571 (JP05102571 Heisei) 19930428
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 94, No. 11
AB PURPOSE: To form a substrate easily and at low cost and radiate the heat of electronic components surely by forming a resin **insulating layer** with a recess, in the region excluding the electronic component **mounting** part on the external surface of a base material, and forming a **metallic layer** in a great part of the surface of the resin **insulating layer**.
CONSTITUTION: A wiring pattern 3a, a **bonding pad** 3b, etc., are formed and a cavity 4 is provided on the surface of a base material 2 constituting a substrate 1 for **mounting** electronic components. An IC chip 5 is accommodated in the cavity 4. And, the **bonding pad** on IC chip side and the **bonding pad** 3b on base material side are electrically connected with each other **through** a bonding **wire** 6. An **insulating layer** 7 made of photosensitive resin as a resin **insulating layer** is made on the rear of the base material 2, and a plurality of holes for formation of interstitial via holes as recesses are formed in the **insulating layer** 7. An electroless copper-plated layer 9 as a **metallic layer** is formed in the great part on the **insulating layer** 7.

L22 ANSWER 7 OF 7 JAPIO COPYRIGHT 2002 JPO
AN 1989-005092 JAPIO

TI CIRCUIT SUBSTRATE FOR HIGH POWER AND HYBRID INTEGRATED CIRCUIT THEREOF
IN KATO KAZUO; NAKANO TATSUO; ASAI SHINICHIRO
PA DENKI KAGAKU KOGYO KK, JP (CO 000329)
PI JP 01005092 A 19890110 Heisei
AI JP1987-161810 (JP62161810 Heisei) 19870629
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 749, Vol. 13, No. 176, P. 9 (19890425)
AB PURPOSE: To stabilize the adhesive property and the dielectric strength property with respect to an **insulating layer** and a copper foil, and to prevent the **insulating layer** from cracking, by superposing an Al foil on the **insulating layer** of a **metallic** substrate and by forming a copper foil with wall thickness on the Al foil.
CONSTITUTION: A **bonding pads** 3 of Al foil etched are formed on an **insulating layer** 5 which is laminated on a metallic substrate 6 of Al or the like. And a copper foil layer 1 with wall thickness of more than 35.mu.m is laminated on each of the bonding posts 3. Moreover, a semiconductor device consisting of a power transistor 7 or the like is **mounted** on a part of the copper foil layer 1 with wall thickness through an eutectic solder 10. The transistor 7 is connected to other bonding post 3 **through** an Al **wire** 9. Therefore, the adhesive strength between the **metallic** foil **layer** and the **insulating layer** increases and being stabilized. Besides, the thermal stress resulting from the difference of expansion coefficient between the metallic substrate and the copper foil is reduced to prevent the **insulating layer** from being damaged without the dielectric strength being lowered.

L26 ANSWER 1 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-049514 [04] WPIX
CR 1992-037022 [05]
DNN N2000-038883
TI Lead connection structure of IC package - has IC pellet on conductive **mounting** material attached to ceramic case base and closed with airtight cap with external wire connecting to IC pellet.
DC U11
PA (NIDE) NEC CORP
CYC 1
PI JP 11312747 A 19991109 (200004)* 3p
ADT JP 11312747 A Div ex JP 1990-84221 19900330, JP 1998-329314 19900330
PRAI JP 1990-84221 19900330; JP 1998-329314 19900330
AB JP 11312747 A UPAB: 20000124
NOVELTY - Package has IC pellet (3) on conductive **mount** material (2) attached to concave part of ceramic case base (1) with surrounding walls and closed airtight by cap (8). External **wire** is drawn **through** gap in wall between case and base by coaxial conductor and connected to IC pellet. On inner wall of cap, a conductive **metal film** (10) is formed. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the lead connection method of IC package.
USE - For IC package.
ADVANTAGE - The design attenuates noise pick-up by shielding provided by coaxial construction and conductor film on inner wall. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of lead connection structure. (1) Ceramic case base; (2) Conductive **mount** material; (3) IC pellet; (8) Cap; (10) Conductive **metal film**.
Dwg.1/4

L26 ANSWER 2 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-484780 [41] WPIX
DNN N1999-361809
TI Scribed area structure in semiconductor device - has metal wiring which is exposed through opening of protection **film** of **metal** wiring pad and is then etched.
DC U11
PA (SHIH) SEIKO EPSON CORP
CYC 1
PI JP 11204525 A 19990730 (199941)* 3p
ADT JP 11204525 A JP 1998-6016 19980114
PRAI JP 1998-6016 19980114
AB JP 11204525 A UPAB: 19991011
NOVELTY - The metal wiring pad (101) forms the lead-out electrode from the circuit of monitor transistor formed on the scribed area. The metal wiring exposed through the opening of the protection film of the pad, is etched.
USE - In semiconductor device.
ADVANTAGE - Prevents short circuiting with a bonding wire or the lead for **mounting** too hastily and generating an electric defect.
DESCRIPTION OF DRAWING(S) - The figure shows sectional view of semiconductor device. (101) Metal wiring pad.
Dwg.1/4

L26 ANSWER 3 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-575020 [49] WPIX
DNN N1998-448192
TI SAW device for high frequency band-pass filter - has pair of comb shaped electrode patterns formed on piezoelectric substrate.
DC U25 V06

PA (HITN) HITACHI DENSHI LTD
CYC 1
PI JP 10256872 A 19980925 (199849)* 6p
ADT JP 10256872 A JP 1997-55650 19970311
PRAI JP 1997-55650 19970311
AB JP 10256872 A UPAB: 19981217
The device has a **metallic film** containing aluminium which is formed on a piezoelectric substrate (1). The **metallic film** is processed to form a pair of comb shaped electrode patterns (2,3).

The piezoelectric substrate is then cut and fixed on a **mounting** package (4). The piezoelectric substrate has several **bonding pads** (5A-5D,6A-6D) connected to respective external terminals (7A-7D,8A-8D) of the **mounting** package **through** bonding **wires** (9A- 9D,10A-10D).

ADVANTAGE - Reduces number of assembling processes. Improves input signal receiving efficiency. Reduces dicing work of piezoelectric substrate. Reduces components such as package cap. Offers superior frequency characteristics.
Dwg.1/4

L26 ANSWER 4 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-134706 [18] WPIX
DNN N1995-106041
TI Semiconductor device manufacturing method - involves face down of **mounting** semiconductor chip on wiring board through two **metal layers** with connection and electrode pads connected electrically.
DC U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 07058114 A 19950303 (199518)* 7p
ADT JP 07058114 A JP 1993-204899 19930819
PRAI JP 1993-204899 19930819
AB JP 07058114 A UPAB: 19950518
The manufacturing method consists of an electrode pad (13) formed on a semiconductor chip (11) and surrounded by a protection **layer** (12). A **metal** barrier **layer** (14) is formed on the electrode pad and has a main field. A solder exclusion film (15) is formed on the main field of the first **metal layer** and is smaller than the main field. A small solder bump (16) is formed on the **metal** barrier **layer**. The solder exclusion film surrounds the periphery of the solder bump. The solder bump is **mounted** on a wiring board (17) through a connection pad (18). Thus the wiring board is **mounted** on the semiconductor chip and the electrode pad and connection pad are connected electrically.

ADVANTAGE - Prevents reduction of intensity and peeling of bump during metal barrier etching. Avoids spreading of bump in horizontal direction and breakage of bump connection part by heat stress. Provides device with high mechanical and electrical reliability.
Dwg.1/21

L26 ANSWER 5 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1993-047827 [06] WPIX
TI Ceramic dual in-line package IC - has each electrode pad of **mounted** chip, linked with thick **metallised layer** of substrate and lead **via** bonded **wire** NoAbstract.
DC U11
PA (SUME) SUMITOMO ELECTRIC CO

CYC 1
PI JP 04370962 A 19921224 (199306)* 3p
ADT JP 04370962 A JP 1991-147536 19910619
PRAI JP 1991-147536 19910619

L26 ANSWER 6 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1990-225044 [30] WPIX
DNN N1990-174646
TI Encapsulated semiconductor using CQFP, FP, DIP ceramics - has **metal layers** coupled by wires to device in ceramic sealed package.
DC U11
IN ALIUS, E; BUHLING, D; LUDEWIG, J; SCHEIBE, H B; WOLDT, G
PA (MIKR-N) VEB FORSCH MIKROEL
CYC 1
PI DD 276185 A 19900214 (199030)*
ADT DD 276185 A DD 1988-320581 19881010
PRAI DD 1988-320581 19881010
AB DD 276185 A UPAB: 19930928
The encapsulated semiconductor arrangement comprises a ceramic subshell (1) with a sink and an encapsulating seal of a glass-soldered ceramic upper shell. A semiconductor (6) is fixed to a **metallisation layer** (2) in the sink, and this is attached to electric carrier strips (4) **via wires** (7).
The **metallisation layer** (2) is of pure aluminium, or aluminium alloy. The layer may be **mounted** on the whole area of the sub-shell (1).
1/1

L26 ANSWER 7 OF 10 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1989-042881 [06] WPIX
DNN N1989-110918 DNC C1989-018763
TI Ceramic package for electronic component - comprises high-heat conductive ceramic and mullite sintering object for low permittivity NoAbstract Dwg 1/1.
DC U11 U14
PA (SHIA) SHINKO DENKI KOGYO KK; (SHIA) SHINKO ELECTRIC CO LTD
CYC 2
PI JP 63314855 A 19881222 (198906)* 5p
US 4827082 A 19890502 (198920)
ADT JP 63314855 A JP 1987-150683 19870617; US 4827082 A US 1988-207218 19880616
PRAI JP 1987-150683 19870617

L26 ANSWER 8 OF 10 JAPIO COPYRIGHT 2002 JPO
AN 1990-186670 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT
IN KOBAYASHI TAMOTSU; NAGAKUBO SHIGEAKI
PA NEC ENG LTD, JP (CO 329822)
PI JP 02186670 A 19900720 Heisei
AI JP1989-6207 (JP01006207 Heisei) 19890113
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 987, Vol. 14, No. 461, P. 90 (19901005)
AB PURPOSE: To reduce power external pins in numbers by a method wherein a power source conductive region is provided to a case, in which a semiconductor chip is **mounted**, surrounding the semiconductor chip, and a connecting wire is provided between the power source conductive region and the power pad of the semiconductor chip.
CONSTITUTION: A GND conductive region 3 and a VDD conductive region 4,

which are for instance **metallized layers** deposited on ceramics, are provided surrounding a semiconductor chip 5, and the regions 3 and 4 are connected to GND and VDD external pins 2 inside a package. In this case, the GND conductive region 3 and the VDD conductive region 4 are made small in impedance from the side of the external pin by making the **metallized layers** thick enough. GND and VDD **bonding pads** of the semiconductor chip 5 are connected to the GND and the VDD conductive region, 3 and 4, at the closest bonding points **through** bonding **wires** respectively. By this setup, when a semiconductor chip which needs a large number of power pads is **mounted**, the power external pins of package can be limited to a minimum in numbers, so that a system can be composed of semiconductor integrated circuits provided with external pins smaller in numbers.

L26 ANSWER 9 OF 10 JAPIO COPYRIGHT 2002 JPO
AN 1989-144641 JAPIO
TI CHIP CARRIER
IN HOSOI YOSHIHIRO
PA KYOCERA CORP, JP (CO 358923)
PI JP 01144641 A 19890606 Heisei
AI JP1987-304125 (JP62304125 Heisei) 19871130
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 817, Vol. 13, No. 4, P. 4 (19890907)
AB PURPOSE: To reduce the generation of conductive rust and discoloration, and to connect a semiconductor element positively and firmly to external electricity by applying a coating layer mainly comprising platinum, palladium or an alloy thereof onto a **metallizing metallic layer** provided to a vessel and applying a **metallic layer** mainly containing gold onto said coating layer in a **bonding pad** section.
CONSTITUTION: A semiconductor element 6 is **mounted** onto the base of a recessed section shaped to an insulating base body 1. A **metallizing metallic layer** 3 composed of W, Mo, etc., is shaped extending over the base from a recessed-section stepped top face, electrodes for the semiconductor element 6 are connected onto the top face of the layer 3 **through wires** 7, and a base section is brazed to wiring conductors 9 in an external wiring substrate 8. A coating layer 4 mainly comprising Pt, Pd or these alloys is applied onto an exposed outside surface. Consequently, clearances are shaped on the side face of the **metallizing metallic layer** 3 and near the surface of the insulating base body 1, and no conductive rust is generated even when moisture, etc., adhere. **Metallic layers** 5 mainly containing gold are attached to **bonding pad** sections 12. The **metallic layer** 5 has low hardness and is chemically stable, thus positively welding the wire 7 and the **metallic layer** 5, then firmly joining them.

L26 ANSWER 10 OF 10 JAPIO COPYRIGHT 2002 JPO
AN 1983-111350 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
IN UENO TATSUAKI
PA HITACHI LTD, JP (CO 000510)
PI JP 58111350 A 19830702 Showa
AI JP1981-209241 (JP56209241 Showa) 19811225
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 200, Vol. 7, No. 2181, P. 108 (19830928)
AB PURPOSE: To enhance reliability of a semiconductor device by **mounting** an IC chip to the dent of ceramic substate through a

metallized layer and by supplying the output of the substrate bias generating circuit of IC to an IC substrate **through** the bonding **wire** and **metallized layer**.
CONSTITUTION: A ceramic substrate 1 having dent 8 is configurated by **stacking** the ceramic plates 5, 6, 7, and an IC chip 2 is fixed to the dent 8 through the nickel layer 11 and gold plated **layer** 12. A **metallized layer** 10 on the ceramic plate 5 and a **metallized layer** 4a on the ceramic plate 6 are connected through a through hole 9. On the **metallized layer** 4a, a **bonding pad** consisting of the nic kel layer 11 and gold plated layer 12 is provided and is connected to the output terminal of substrate bias generating circuit on the chip 2 **through** the bonding **wire** 3. Thereby, the substrate of chip 2 and substrate bias output are connected electrically. Manufacturing is very simplifed and high reliability is obtained.

L34 ANSWER 1 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-061610 [07] WPIX
DNN N2001-046176 DNC C2001-017129
TI Interface device for providing an interface between testing equipment and an integrated circuit to be tested, includes contact end of each elongate member extending through a respective aperture in a guide member body member.
DC L03 S01 U11
IN SAWHILL, R A; SHAH, P I
PA (SPIR-N) SPIRE TECHNOLOGIES PTE LTD
CYC 85
PI WO 2000074108 A2 20001207 (200107)* EN 16p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
AU 9940674 A 20001218 (200118)
ADT WO 2000074108 A2 WO 1999-SG48 19990528; AU 9940674 A AU 1999-40674 19990528, WO 1999-SG48 19990528
FDT AU 9940674 A Based on WO 200074108
PRAI WO 1999-SG48 19990528
AB WO 200074108 A UPAB: 20010202
NOVELTY - An interface device comprises a body member, elongate contact members, and a body portion, and a guide member with apertures. Each contact member has a contact end extending through the aperture. The width of the contact end is less than that of the aperture to permit lateral movement of each contact end within the respective aperture.

DETAILED DESCRIPTION - An interface device comprises a body member; elongate contact members, each comprises a contact end (13) adapted to contact a **bond pad** of an integrated circuit to be tested, and a body portion (10) coupled to the body member; and a guide member **mounted** on the body member. The guide member (3) comprises a planar member with apertures. The contact end of each elongate member extends through a respective aperture in the guide member. The width of each contact end is less than that of the respective aperture to permit lateral movement of each contact end within the respective aperture. An INDEPENDENT CLAIM is also included for a method of forming a through bore in a piece of material, comprising generating a **parallel** beam of coherent light; illuminating an object having a circular cross section with a diameter less than that of the beam with the **parallel** beam to form an annular beam; and focusing the annular beam into the piece of material so that the annular beam incident on the piece of material has an external diameter corresponding to that of the desired through bore to burn away a corresponding annular piece of material to form the through bore.

USE - For providing an interface between testing equipment and an integrated circuit to be tested.

ADVANTAGE - As the contact end of each elongate member extends through a respective aperture in the guide member, the guide member limits lateral displacement of the contact ends. This permits thinner diameter wire to be used for the pins (5) which enables higher pitch densities for the pins to be achieved while still maintaining the lateral position of the contact ends.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a portion of the interface device.
Guide member 3

Pins 5
Body portion 10
Contact end 13
Dwg.2/3

L34 ANSWER 2 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-559719 [48] WPIX
DNN N1998-436492
TI Reinforcing system for **bond pad** - has at least one dielectric layer positioned under **bond pad** with patterned reinforcing structure positioned in dielectric layer.
DC U11
IN MARTIN, C A; SARAN, M
PA (TEXI) TEXAS INSTR INC
CYC 29
PI EP 875934 A2 19981104 (199848)* EN 8p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11054544 A 19990226 (199919) 27p
KR 98086680 A 19981205 (200009)
TW 370710 A 19990921 (200036)
US 6143396 A 20001107 (200059)
ADT EP 875934 A2 EP 1998-303365 19980430; JP 11054544 A JP 1998-158308 19980430; KR 98086680 A KR 1998-15484 19980430; TW 370710 A TW 1998-106650 19980515; US 6143396 A US 1997-847239 19970501
PRAI US 1997-847239 19970501
AB EP 875934 A UPAB: 19981203
The reinforcing system (10) for a **bond pad** (12) includes at least one dielectric layer (20,22) positioned under the **bond pad**. A patterned reinforcing structure (30) is positioned in the dielectric layer. The dielectric layer includes a weak organic dielectric layer. The patterned reinforcing structure is constructed of reinforcing lines of a material stronger than the dielectric layer. The patterned reinforcing structure is constructed of interconnecting **metallisation lines**.

The dielectric layer is at least one multi-layered dielectric **stack**. The patterned reinforcing structure occupies a substantial area under the **bond pad**. The patterned reinforcing structure includes vacant areas filled by the dielectric layer. The patterned reinforcing structure includes a grid pattern, a repeated crucifix pattern or a honeycomb pattern. The patterned reinforcing structure includes alternate layers with **parallel** lines perpendicular to one another.

ADVANTAGE - Minimises probe and **bonding pad** failure caused by weak dielectric layer.
Dwg.1/11

L34 ANSWER 3 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1997-558281 [51] WPIX
DNN N1997-465362 DNC C1997-178193
TI Apparatus for testing integrated circuit chip including **bonding pads** prior to assembly - has contacts arranged in predetermined pattern, polymeric substrate over conductors with conductor springs between surfaces and non-conductive plate onto which chip is pressed.
DC A85 L03 S01 U11
IN LEE, S W
PA (NASC) NAT SEMICONDUCTOR INC
CYC 1
PI US 5686842 A 19971111 (199751)* 6p

ADT US 5686842 A US 1995-521619 19950831
PRAI US 1995-521619 19950831
AB US 5686842 A UPAB: 19990210
An apparatus for testing an integrated circuit chip including **bonding pads** in a predetermined pattern, prior to **mounting** on a package, comprises (i) a number of contacts arranged in the predetermined pattern; (ii) a substrate over the conductors, having opposed first and second surfaces and including many conductors extending between the first surface which is **mounts** on the contacts, and the second surface; and (iii) a non-conductive plate **mounted** on the second surface, having a number of openings arranged in the predetermined pattern. When the integrated circuit chip is pressed against the non-conductive plate, at least one of the conductors protrudes through each opening and contacts one of the **bonding pads** to provide an electrical connection between each of the contacts and an associated one of the **bonding pads**.

Also claimed is the method of testing an integrated circuit chip prior to **mounting** on a package.

Preferably, the non-conductive plate is a ceramic or a glass. The substrate comprises a silicone rubber wafer defining the first and second surfaces, and including many **parallel metal wires** extending between the first and second surfaces.

USE - Used for testing integrated circuit chips before assembly.

ADVANTAGE - The apparatus provides low cast, known good die testing of flip chips prior to **mounting** on direct chip attach packages.

Dwg.3/4

L34 ANSWER 4 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1997-297455 [27] WPIX
DNN N1997-245812
TI Multi-chip module for e.g. computer system - has moulded template with intercommunicating chambers each containing round stage on bottom of chamber with heat able to flow between stages.
DC U11 U14
IN HSU, C
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 5633530 A 19970527 (199727)* 6p
ADT US 5633530 A US 1995-547555 19951024
PRAI US 1995-547555 19951024
AB US 5633530 A UPAB: 19970702
The semiconductor multi-chip module configuration includes a module template (10) with an interior portion and at least two chambers (I,II) made of either ceramic or plastic, which communicate with each other and are arranged vertically in the interior portion. Heat is allowed to flow between the stages. Several **parallel** pins extend outwardly from the module template. There is a round stage (11a,11b) at the bottom of each chamber. Several leadframes (12a,12b) are formed over each stage and connected to predetermined **parallel** pins (20).

A support member (15a,15b) is formed around the upper end of each chamber. There are at least two semiconductor chips with predetermined circuits and conductive pads. Each chip is adhered to a respective one of the stages. **Metal wires** made of either gold or aluminium, connect the conductive pads of each chip with corresponding leadframes. There is a thermally conductive metal covering plate (16a,16b) for each chamber sealed on its respective support member.

ADVANTAGE - Improves heat dissipation due to separation between **stacked** chips.

Dwg.1/2

L34 ANSWER 5 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1996-293512 JAPIO
TI RESIN-SEALED SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN NAKANO HIDEKI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 08293512 A 19961105 Heisei
AI JP1995-96369 (JP07096369 Heisei) 19950421
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 11
AB PURPOSE: To prevent a wire from breaking due to resin peeling during reflow of a resin-sealed semiconductor device by bonding a **metallic** fine **wire parallel** to a plane of a lead in an end part of a lead enclosed with a pellet and resin. CONSTITUTION: A semiconductor pellet 2 wherein a semiconductor element is formed is **mounted** on a bed 3 consisting of a plate of 42 alloy/copper material through an adhesive 5. A capillary 6 threading wire 4 consisting of a gold wire is descended to a specified region wherein a **bonding pad** is formed on the semiconductor pellet 2 and an end part 1 (ball part) of the wire 4 is bonded to the semiconductor pellet 2. The capillary 6 is moved to a bed side end part of a lead 7 while discharging the gold wire 4 from the capillary 6. The lead 7 is formed by applying silver plating to a 42 alloy/copper material. Furthermore, the capillary 6 is moved **parallel** to a lead plane from an end part of the lead 7 and the wire 4 is bonded **parallel** from an end part of the lead 7.

L34 ANSWER 6 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1993-211191 JAPIO
TI INTEGRATED CIRCUIT DEVICE
IN SASAKI CHIHIRO
PA NEC CORP, JP (CO 000423)
PI JP 05211191 A 19930820 Heisei
AI JP1991-303669 (JP03303669 Heisei) 19911120
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1468, Vol. 17, No. 649, P. 31 (19931202)
AB PURPOSE: To decrease defective assembly, by so providing a stitch land as to be **parallel** with the wiring direction of a **metallic wire**, in the device wherein a plurality of stitch lands are provided around a semiconductor pellet and they are respectively connected with the semiconductor pellet by the **metallic wires**. CONSTITUTION: In a hybrid integrated circuit device, the shape of a stitch land 4, which is provided at the end part of a wiring pattern 5 formed on a board, is so formed as to be **parallel** with the wiring direction of a bonding wire 3. When another **mounting** parts 6 is provided just near an IC pellet 1, the stitch land 4 can not be provided in lateral proximity to a **bonding pad** 2 formed on the IC pellet 1 and it is made distant from the **bonding pad** 2. Even in the state wherein the wiring direction of the bonding wire 3 is made oblique, by using the foregoing stitch land 4, the drawback that the bonding wire 3 and the stitch land 4 adjacent to it are short-circuited can be eliminated.

L34 ANSWER 7 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1991-066149 JAPIO
TI SEMICONDUCTOR DEVICE
IN HIROSE MASAHIRO; FUNAKOSHI HARUO
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 03066149 A 19910320 Heisei

AI JP1989-203158 (JP01203158 Heisei) 19890804
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1076, Vol. 15, No. 229, P. 44 (19910611)
AB PURPOSE: To prevent moisture from entering into a semiconductor element in a short time by a method wherein a metal lead used to input/output a signal from the semiconductor element and inside and outside parts and a **metal wire** used to connect the lead to the semiconductor element to obtain a continuity are sealed with a resin.
CONSTITUTION: Leads 3 interlinked respectively to outer frames 7 toward a line connecting midpoints of two section bars 8 are extended at right angles to the outer frames 7. The leads 3 extended from the upper and lower outer frames 7 are arranged and installed alternately and in **parallel** at definite intervals in the central part of the upper and lower outer frames 7. Inner leads 3b in prescribed parts on which a semiconductor element 1 is **mounted** in nearly the central part of the outer frames 7 and the section bars 8 are coated with an insulating layer 10; the semiconductor element 1 is **mounted** in the central part of the insulating layer 10. A **bonding pad** 6 on the **mounted** semiconductor element 1 is bonded to one end of a wire 4; on the other hand, the inner leads 3b existing so as to be adjacent to the **bonding pad** 6 in its opposite position are bonded to the other end of the wire 4; this assembly is resin-sealed with a sealing material 5.

L34 ANSWER 8 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1988-056466 JAPIO
TI **MOUNTING** OF DRIVER IC ON THERMAL HEAD
IN SUZUKI MASABUMI
PA OKI ELECTRIC IND CO LTD, JP (CO 000029)
PI JP 63056466 A 19880311 Showa
AI JP1986-199024 (JP61199024 Showa) 19860827
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: M, Sect. No. 725, Vol. 12, No. 274, P. 26 (19880729)
AB PURPOSE: To reduce the wiring area of a driver IC and also manhours by arranging signal pads of a driver IC to be **mounted** on two sides opposed to an adjoining driver IC symmetrically to the right and left, and directly wire-bonding each other IC chips which are multi-**mounted** on a single line.
CONSTITUTION: Signal patterns I-IV of a substrate are directly wire-**bonded** to signal **pads** 1-6 of IC1 with fine **metallic wire** 11. further, IC2 of the next stage is provided adjacent to the IC1, and at the same time, signal pads 1-6 of the IC2 are wire-bonded directly to signal pads 1'-6' of the IC1 respectively with fine **metallic wire** 11. The case is the same with the wire-bonding between the IC2 and IC3. The signal is entered into the signal pads 1-6 of the IC1 from substrate patterns I-VI, and is transferred to the IC2 of the next stage. The same signal pads are to be arranged so that the signal pads 1'-6' and 1-6 may be **parallel** to allow no wire crossing each other when adjoining driver ICs are wire-bonded.

L35 ANSWER 1 OF 6 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-462601 [50] WPIX
TI Wafer level **stack** package and method for making the same.
DC U11
IN KIM, J M; PARK, C J
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2001004547 A 20010115 (200150)* 1p
ADT KR 2001004547 A KR 1999-25237 19990629
PRAI KR 1999-25237 19990629
AB KR2001004547 A UPAB: 20010905
NOVELTY - A wafer level **stack** package and a method for making the same are provided to make one package by **stacking** at least two semiconductor chips, and enhance an electric conductive performance by reducing an electric signal transmission path.
DETAILED DESCRIPTION - A wafer level **stack** package includes upper/lower semiconductor chip, a lower **insulating layer** (31), upper/lower metal pattern(40,41), an upper **insulating layer**(50,51), a via hole, a pattern film(70), and a solder ball(90). Each **bonding pad** is arranged to face an upper part of the semiconductor chip. The lower **insulating layer** is deposited on the semiconductor chip in order to expose the **bonding pad**. The metal pattern is deposited on the lower **insulating layer**, its one end is connected to each **bonding pad**, and the other end extends to an edge of each semiconductor chip. The upper **insulating layer** is deposited on each lower **insulating layer**. Some part of the upper **insulating layer**, deposited on the lower **insulating layer**, is faced to the bottom of the upper semiconductor chip. The via hole is formed to every outer part of the upper semiconductor chip positioned on the other end of the lower metal pattern, and exposes the other end of the upper/lower metal pattern. The pattern film is **mounted** on the upper **insulating layer** deposited on the upper semiconductor chip, a **metal line** is arranged in the **insulating layer**, one end of the **metal line** is exposed **through** a side of the **insulating layer**, the other end of the **metal line** is exposed **through** a surface of the **insulating layer**, thereby a ball land is formed, and one end of the **metal line** is connected electrically to each **bonding pad** by a pair of **metal wire**. The solder ball is moutned to a ball land of the pattern film. Thereby, the wafer level **stack** package makes one package by **stacking** at least two semiconductor chips, and enhances an electric conductive performance by reducing an electric signal transmission path.
Dwg.1/10

L35 ANSWER 2 OF 6 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-055570 [07] WPIX
DNN N2001-043075
TI Semiconductor device manufacturing method e.g. for semiconductor chip, involves removing connection piece from connection portion to separate semiconductor integrated circuit.
DC U11
PA (SAOL) SANYO ELECTRIC CO LTD
CYC 1
PI JP 2000315700 A 20001114 (200107)* 6p

ADT JP 2000315700 A JP 1999-122076 19990428
PRAI JP 1999-122076 19990428
AB JP2000315700 A UPAB: 20010202
NOVELTY - A frame is **mounted** on wafer so that **bonding pad** and connection piece (4) of wafer which are connected to each other **through metal** thin **line**, are in accord and **insulated** resin **layer** is coated on the wafer surface. A connection piece is removed from the connection portion (5) to separate a semiconductor integrated circuit.
DETAILED DESCRIPTION - The connection piece is present inside a **bonding pad** with respect to **bonding pad** of semiconductor integrated circuit. The connection pieces are fixed to connection portion in the shape of a matrix.
USE - For manufacturing channel substrate planar semiconductor device e.g. semiconductor chip.
ADVANTAGE - Ceramic substrate is omitted, hence size and cost of semiconductor device are reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the semiconductor device manufacturing method.
Connection piece 4
Connection portion 5
Dwg.2/4

L35 ANSWER 3 OF 6 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-319233 [27] WPIX
DNN N1999-239449
TI Flip-chip **mounting** structure of semiconductor device - interposes aluminum ball between **insulating layer** and broad substrate electrode **through** aluminum **wire**.
DC U11
PA (SONY) SONY CORP
CYC 1
PI JP 11111770 A 19990423 (199927)* 11p
ADT JP 11111770 A JP 1997-268271 19971001
PRAI JP 1997-268271 19971001
AB JP 11111770 A UPAB: 19990719
NOVELTY - A semiconductor chip (10) is **mounted** on the **insulating layer** (14), which has a chip electrode (12). To the tip electrode, an Al ball (22) is connected **through** the Al **wire** (24). The aluminum wire also connects the lower end of the ball to the substrate electrode (18) of a wiring board (16), and the upper end of the ball is connected to the **insulating layer** (14). DETAILED DESCRIPTION - The space between the semiconductor chip and the wiring board is 60-70 mu m. The diameter of the Al ball is 80 mu m. The diameter of the Al wire is 30 mu m. An INDEPENDENT CLAIM is also included for flip-chip **mounting** method of semiconductor device.
USE - For flip-chip **mounting** of semiconductor device on circuit board.
ADVANTAGE - Since the aluminum ball with larger diameter is interposed, resistivity to oppose the heat during flip-chip **mounting** is increased. With **metal wire** between the **metal** ball and electrode, the stress generated due to the difference in the coefficient of linear expansion of a semiconductor chip and circuit board is greatly absorbed, thus increasing the reliability of the semiconductor device and throughput is increased. DESCRIPTION OF DRAWING(S) - The figure depicts the sectional view of the semiconductor device. (10) Semiconductor chip; (12) Chip electrode; (14) **Insulating layer**; (16) Circuit wiring board; (18)

Substrate electrode; (22) Aluminum ball; (24) Aluminum wire.
Dwg.1/18

L35 ANSWER 4 OF 6 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1996-214761 [22] WPIX
DNN N1996-180186
TI Semiconductor device - has rotor which is connected to lead part **through metal wire** and is held to specific potential, wherein semiconductor element is **mounted** on lead frame.
DC U11
PA (NIDE) NEC CORP
CYC 1
PI JP 08078610 A 19960322 (199622)* 9p
ADT JP 08078610 A JP 1994-230433 19940831
PRAI JP 1994-230433 19940831
AB JP 08078610 A UPAB: 19960604
The device includes rotor contact (22,32) formed respectively through the **insulated layers** (21,31) and to the lead vertical surface. The rotor is connected to a lead with a **metal wire** and is held to a specific potential. The semiconductor element is **mounted** on a lead frame (10).
ADVANTAGE - Improves noise immunity. Controls signal wave interference. Widens semiconductor device application. Increases flexibility and reduces **insulated layer** thickness.
Dwg.1/12

L35 ANSWER 5 OF 6 JAPIO COPYRIGHT 2002 JPO
AN 1999-135663 JAPIO
TI MOLDED BGA TYPE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN KIMURA NAOTO
PA NEC KYUSHU LTD, JP (CO 423996)
PI JP 11135663 A 19990521 Heisei
AI JP1997-295305 (JP09295305 Heisei) 19971028
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 5
AB PURPOSE: TO BE SOLVED:To reduce material cost for a wire bonding to produce at a low cost and facilitate bonding with **metal** thin **wires** to solder balls by providing conductive **layer** on an **insulative** resin **film** of a chip.
CONSTITUTION: nufacturing method comprises the steps of forming an **insulative** resin **film** 3 on at least a part of the surface of a semiconductor chip except pads 2, forming a conductive layer 4 over regions at least including regions corresponding to solder ball 6 **mounting** positions on the resin film 3, **bonding** the **pads** 2 to the conductive layer 4 **through wires** 5 on this layer 4, encapsulating a chip 1 with a resin, boring holes 9 into encapsulated resin 7 so as to expose a part of the **wire** -bonded **metal** thin **wires** 5 and **mounting** the solder balls 6 in the holes 9. This reduces the material cost for the wire bonding to enable manufacture at a low cost and facilitates bonding with the **metallic** thin **wires** 5 to the solder balls 6.

L35 ANSWER 6 OF 6 JAPIO COPYRIGHT 2002 JPO
AN 1991-204965 JAPIO
TI RESIN-SEALED SEMICONDUCTOR DEVICE
IN MATSUKURA TAKUMI
PA NEC CORP, JP (CO 000423)
PI JP 03204965 A 19910906 Heisei

AI JP1990-272563 (JP02272563 Heisei) 19901011

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1140, Vol. 15, No. 476, P. 50 (19911204)

AB PURPOSE: To improve a semiconductor device of this design in degree of integration without changing its resin sealed part in outside dimension by a method wherein leads are fixed to the upside of a semiconductor element through the intermediary of an insulating adhesive agent, and the leads and a **bonding pad** are connected together **through** a **metal wire**.

CONSTITUTION: A semiconductor element **mounting** section is not provided to a lead frame, an inner lead 5 is made to overlap the upside of a semiconductor element 1 on which a circuit has been formed, and an insulating adhesive agent 3 provided to the underside of the wide tip of the inner lead 5 is bonded to the upside of the semiconductor element 1 to fix the inner leads 5 to the semiconductor element 1. A **metal wire** 7 is bonded to a **bonding pad** 8 on the semiconductor element 1 and the wide tips of the inner leads 5 and 5a which serve as **metal wire** connecting parts, and a resin sealed part 9 is sealed up with epoxy resin excluding outer leads. As an **insulating film** 4 is pasted on the upside of the inner lead 5a, the **metal wire** 7 is prevented from being shortcircuited to the inner lead 5a even if the wire 7 is laid striding the inner lead 5a.

L36 ANSWER 1 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-583933 [55] WPIX
DNN N2000-432616
TI Chip size package type semiconductor device for portable personal computer, has semiconductor chip comprising electrode electrically connected to wiring layer **through wire**.
DC U11
PA (HITW) HITACHI HOKKAI SEMICONDUCTOR; (HITA) HITACHI LTD
CYC 1
PI JP 2000236040 A 20000829 (200055)* 20p
ADT JP 2000236040 A JP 1999-36142 19990215
PRAI JP 1999-36142 19990215
AB JP2000236040 A UPAB: 20001102
NOVELTY - Pads (3,3A,3B) provided inside tetragon-like wiring board (1) along peripheral surface electrically connect the board with wiring layer (2). Semiconductor chip provided on **insulating film** (6) of the wiring board, has electrode (8) connected to the wiring layer **through wire** (10).
USE - Chip size package or chip scale package (CSP) type semiconductor device with face-up structure for portable telephone, portable information processing terminal device, portable personal computer.
ADVANTAGE - Smaller semiconductor chips can be **mounted** on wiring board without degrading the electrical property. Improves semiconductor device manufacturing yield without degrading electrical property.
DESCRIPTION OF DRAWING(S) - The figure shows the principal-part sectional view of CSP type semiconductor device.
Wiring board 1
Wiring layer 2
Pad 3,3A,3B
Insulating film 6
Electrode 8
Wire 10
Dwg.8/24

L36 ANSWER 2 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2000-248747 [22] WPIX
DNN N2000-186312 DNC C2000-075427
TI Bonding wire **mounting** structure in resin sealed semiconductor device - has contact pads in wiring layer, which obstructs through-hole, such that bonding wire connects each electrode terminal and contact pad.
DC A85 L03 U11
PA (TOKE) TOSHIBA KK; (TOSZ) TOSHIBA MICROELECTRONICS KK
CYC 1
PI JP 11354673 A 19991224 (200022)* 9p
ADT JP 11354673 A JP 1998-158008 19980605
PRAI JP 1998-158008 19980605
AB JP 11354673 A UPAB: 20000522
NOVELTY - **Insulated** resin **film** (5) has several through-holes (6,7) and external connecting terminal. A wiring layer (8) has several contact pads which obstruct the through-holes. A bonding wire (11) connects each electrode terminal and contact pads. A resin sealing layer (12) is coated on the assembly.
USE - In resin sealed semiconductor device.
ADVANTAGE - As molding of a lead frame is not needed, cost is reduced. The semiconductor device has heat release property and

lightweight. DESCRIPTION OF DRAWING(S) - The figure shows the sectional vie of resin sealed semiconductor device. (5) **Insulated** resin **film**; (6,7) Through-holes; (8) Wiring layer; (11) Bonding wire; (12) Resin sealing layer.
Dwg.2/7

L36 ANSWER 3 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-273645 [23] WPIX
DNN N1999-205203
TI Lead frame connection structure of semiconductor device - has inner lead of lead frame connected to electrode of semiconductor device which is **mounted** below heat sink, by passing bonding **wire** **through** opening of heat sink.
DC U11
PA (KYUN) NEC KYUSHU LTD
CYC 1
PI JP 11087594 A 19990330 (199923)* 6p
ADT JP 11087594 A JP 1997-238626 19970903
PRAI JP 1997-238626 19970903
AB JP 11087594 A UPAB: 19990616
NOVELTY - A semiconductor device (7) is **mounted** to lower surface of heat sink (4) which is connected from lower end portion with inner lead (3) through an **insulating** **film** (15). The electrode (16) of the semiconductor device is connected to the inner lead by a bonding **wire** (6) passed **through** opening of heat sink.
USE - For semiconductor device.
ADVANTAGE - Since the bonding wire is supporting using heat sink, the limitation of wire length at time of assembly is unnecessiated. Heat dissipation characteristic is doubled as semiconductor device has structure to attach heat sink on both sides of its surface. DESCRIPTION OF DRAWING(S) - The figure shows sectional view of semiconductor device using lead frame. (3) Inner lead; (4) Heat sink; (6) Bonding wire; (7) Semiconductor device; (15) **Insulating** **film**; (16) Electrode.
Dwg.2/9

L36 ANSWER 4 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-201170 [17] WPIX
DNN N1999-148997
TI Chip size package **mounting** structure on PCB - has IC chip connected to PCB through wirings, bump, external connecting terminal and solder ball, which are inturn fixed on PCB by polyamide **layer** **insulating** adhesive agent and wiring tape.
DC U11
PA (RICO) RICOH KK
CYC 1
PI JP 11045908 A 19990216 (199917)* 6p
ADT JP 11045908 A JP 1997-215544 19970725
PRAI JP 1997-215544 19970725
AB JP 11045908 A UPAB: 19990503
NOVELTY - An IC chip (1) with a **bonding** **pad** (17), is connected to printed board electrode (11) on a PCB through wirings (21,39), a bump (33), an external connecting terminal (31) and a solder ball (43). The conductive materials are fixed on PCB (9) by two polyamide layers (19,23), an insulating adhesive agent (41) and a wiring tape (29).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for CSP **mounting** method .
USE - None given
ADVANTAGE - Pad for external connection can be prepared in arbitrary

position. Generation of crack at junction part is avoided. Since metal bump is connected with the pad for external connection through a conductive paste, the stress exerted on the pad is released. DESCRIPTION OF DRAWING(S) - The figure shows sectional drawing of chip **mounting** structure on PCB. (1) IC chip; (9) PCB; (11) Printed board electrode; (17) **Bonding pad**; (21,39) Wirings; (29) Wiring tape; (41) Adhesive agent; (43) Solder ball.
Dwg.5/5

L36 ANSWER 5 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-487209 [42] WPIX
DNN N1998-380752 DNC C1998-147026
TI Multilayer wiring board for semiconductor device package - has through hole conductor embedded in hole of **insulating layer** through which adjacent wiring conductor layers are connected.
DC A85 L03 U11 V04
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 10209638 A 19980807 (199842)* 7p
ADT JP 10209638 A JP 1997-8752 19970121
PRAI JP 1997-8752 19970121
AB JP 10209638 A UPAB: 19981021
The board comprises an organic resin **insulating layer** (2) and thin film wiring conductor layer (3) which are laminated alternately on the surface of a substrate (1). The adjacent conductor layers are connected mutually through a conductor (6) formed in the hole of **insulating layer**.
A **bonding pad** (7) is formed on the uppermost conductor layer (3), an electronic component (A) is **mounted** on the **bonding pad**. The exposure surface of the uppermost **insulating layer** satisfies the relation 0.05 micrometer=<Ra= <5 micrometer, where Ra is the center line average coarse.
USE - For hybrid IC.
ADVANTAGE - Forms high density wiring. Prevents generation of peeling between organic resin **insulating layer**.
Dwg.1/3

L36 ANSWER 6 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-136646 [13] WPIX
DNN N1998-108470
TI Small outline type semiconductor memory IC package - has conductor leads for signal lines which are electrically connected to each electrode part.
DC U11
PA (TEXI) NIPPON TEXAS INSTR KK
CYC 1
PI JP 10012804 A 19980116 (199813)* 7p
ADT JP 10012804 A JP 1996-184051 19960625
PRAI JP 1996-184051 19960625
AB JP 10012804 A UPAB: 19980330
The package **mounts** a chip (2) on which multiple electrode pads (2a) are formed in rows. A pair of conducting leads (6,7) provided with a respective bus bars (6a,6b,7a,7b) are connected to respective power supply terminals (Vss, Vcc).
The first conducting leads are connected to predetermined electrode pads **through** a conducting **wire** (5). Multiple conducting lead (4) for signal lines are also electrically connected to each electrode pads, electrically.
ADVANTAGE - Increases manufacturing efficiency. Prevents crack or curvature of semiconductor chip by reducing thermal stress applied to

chip. Reduces bonding area of leads. Prevents short circuit between conductor wires, by providing **insulating layer** on leads.
Dwg.1/7

L36 ANSWER 7 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-107308 [10] WPIX
DNN N1998-086289
TI Semiconductor device - has through-hole which is formed on opposite surface side of **insulated film**.
DC U11
PA (SHIA) SHINKO DENKI KOGYO KK
CYC 1
PI JP 09330943 A 19971222 (199810)* 5p
ADT JP 09330943 A JP 1996-152177 19960613
PRAI JP 1996-152177 19960613
AB JP 09330943 A UPAB: 19980309
The device has a wiring pattern film (16) which is **mounted** with a semiconductor device (22). A wiring pattern (14) is formed on the whole surface side of an **insulated film** (10). A connection pad (24) of the semiconductor device and a **bonding pad** (17) of the wiring pattern are connected electrically **through** a **wire** (26).
A through-hole (32) is formed on the opposite surface side of the **insulated film**. The rear side of the **bonding pad** to which the wire is connected is exposed to the hole part.
ADVANTAGE - Improves wire bonding reliability.
Dwg.2/5

L36 ANSWER 8 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1997-218864 [20] WPIX
DNN N1997-180841
TI Ball grid array type semiconductor device e.g. IC, LSI - has lead frame conductor circuit pattern formed between first and second **insulated layers** through etching or press stamping processes.
DC U11
PA (MIHI) MITSUI HIGH TEC KK
CYC 1
PI JP 09064225 A 19970307 (199720)* 6p
JP 3115807 B2 20001211 (200101) 5p
ADT JP 09064225 A JP 1995-240909 19950825; JP 3115807 B2 JP 1995-240909 19950825
FDT JP 3115807 B2 Previous Publ. JP 09064225
PRAI JP 1995-240909 19950825
AB JP 09064225 A UPAB: 19970516
The device (10) has a semiconductor chip (16) **mounted** on the surface of a semiconductor chip **mounting** substrate (14) which includes a conductor circuit pattern (13). Several conductor leads (11) and electrode pads (17) formed on the semiconductor chip surface, are connected **through** bonding **wire** (18). A dense sealing resin element (19) is provided on the side of the semiconductor chip **mounting** surface. A first **insulated layer** (23) provides a first opening (22) which exposes a wire **bonding pad** (21) and a semiconductor chip **mounting** stage (12).
A second **insulated layer** (26) provides a conducting hole (25) which exposes an external connection terminal island (24). The conductor circuit pattern of a lead frame is formed between the first and second **insulated layers** through press

stamping or etching processes.
ADVANTAGE - Reduced manufacturing cost by maintaining shape and size of conductor lead pattern during early stages of manufacturing process. Protects conductor circuit pattern from deformation or chemical damage by coating conductor circuit pattern with resistant mask layer.
Dwg.1/3

L36 ANSWER 9 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1996-418227 [42] WPIX
DNN N1996-352480
TI Semiconductor device for data processor e.g. computer - has several external lead terminals connected to wiring **layer** of **insulated** base using ultrasonic junction.
DC U11
PA (KYOC) KYOCERA CORP
CYC 1
PI JP 08204109 A 19960809 (199642)* 4p
JP 3181008 B2 20010703 (200139) 4p
ADT JP 08204109 A JP 1995-10601 19950126; JP 3181008 B2 JP 1995-10601 19950126
FDT JP 3181008 B2 Previous Publ. JP 08204109
PRAI JP 1995-10601 19950126
AB JP 08204109 A UPAB: 19961021
The device has an insulated base (1) with a wiring layer (4) that has an Al **mounting** area (1a) arranged at its centre. A semiconductor component (3) is **mounted** on the **mounting** area by connecting its electrodes to the wiring layer **through** several bonding **wires** (5).
Several external lead terminals (2) for external connection are attached to the wiring **layer** of the **insulated** base by using an ultrasonic junction. The whole surface of the insulated base and the semiconductor component is covered by a mould resin (6) leaving only some portions of the external lead terminals exposed.
ADVANTAGE - Provides reliable electric connection and improves mechanical strength of external lead terminals. Prevents deformation of external lead even if large power is applied.
Dwg.1/1

L36 ANSWER 10 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-152586 [20] WPIX
DNN N1995-120023 DNC C1995-070623
TI Semiconductor device mfr. with good adhesion between **insulation film** and wiring - by forming **bonding pad** on upper wiring, part being exposed through opening and surface protection film which covers upper wiring and inter-**layer insulating film**.
DC L03 U11
IN HAYASHI, ; YAMANAKA, M; HAYASHI, J
PA (NIDE) NEC CORP; (NIDE) NIPPON DENKI KK
CYC 3
PI JP 07078821 A 19950320 (199520)* 12p
US 5523626 A 19960604 (199628) 18p
US 5994214 A 19991130 (200003)
KR 145649 B1 19981102 (200028)
ADT JP 07078821 A JP 1993-222959 19930908; US 5523626 A US 1994-301621 19940907; US 5994214 A Div ex US 1994-301621 19940907, Cont of US 1995-474904 19950607, US 1997-791066 19970129; KR 145649 B1 KR 1994-22648 19940908
FDT US 5994214 A Div ex US 5523626
PRAI JP 1993-222959 19930908

AB JP 07078821 A UPAB: 19950530
The semiconductor device manufacturing method involving forming a field **oxide film** (102) on a selective portion on the surface of a silicon substrate (101). A lower wiring layer is formed on the surface of the silicon substrate. An inter-**layer insulating film** (131) which has a contact hole (136) is formed on the predetermined part of the lower wiring layer.

A first titanium nitride film (141a), a titanium film (142), a second titanium nitride film (141b) and an aluminium alloy film (143) are layered on the upper face of the inter-**layer insulating film**. An upper wiring which has a **bonding pad** part (156) is formed. A surface protection film (151) covers the inter-**layer insulating film** and the upper wiring. A titanium silicide film (144) is layered inside the contact hole.

ADVANTAGE - Reduces contact resistance of upper wiring and lower wiring layer. Provides good adhesion between inter-**layer insulation film** and upper wiring.
Dwg.1/11

L36 ANSWER 11 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1994-361573 [45] WPIX
DNN N1994-283447
TI Semiconductor device with LOC structure - uses semiconductor chip consisting of many pads which is connected to bus bar and leads **through** bonding **wires**.
DC U11
PA (MITQ) MITSUBISHI ELECTRIC CORP
CYC 1
PI JP 06283659 A 19941007 (199445)* 4p
ADT JP 06283659 A JP 1993-66763 19930325
PRAI JP 1993-66763 19930325
AB JP 06283659 A UPAB: 19950102
The semiconductor device consists of a semiconductor chip (1). The semiconductor chip consists of many leads (4) which is placed through an **insulating film**. The leads are connected directly with a bus bar (3).

The semiconductor chip is also provided with many pads (2). The pads are connected with leads and the bus bar **through** bonding **wires** (5,6).

ADVANTAGE - Improves reliability. Provides high density **mounting** of large scale integration.
Dwg.1/7

L36 ANSWER 12 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1994-120170 [15] WPIX
DNN N1994-094128
TI Integrated circuit chip carrier esp. for IC module package - uses single multiple printed circuit board resin fibre-glass composite material layers, with e.g. IC solder ball connection, and includes inter-level vias and multiple wiring plane' wiring traces for IC connection to carrier pads.
DC U11 U14 V04
IN GAUDENZI, G J; NIHAL, P
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 5
PI EP 592022 A1 19940413 (199415)* EN 10p
R: DE FR GB
US 5313366 A 19940517 (199419) 8p
JP 06112271 A 19940422 (199421) 6p

ADT EP 592022 A1 EP 1993-202299 19930804; US 5313366 A US 1992-929631 19920812; JP 06112271 A JP 1993-161625 19930630
PRAI US 1992-929631 19920812
AB EP 592022 A UPAB: 19940531
The IC carrier includes a carrier connector for power and signal supply to the carrier pref. carrier pads with deposited solder balls. One or more ICs are **mounted** fixed on the carrier pref. by chip **bonding pads** with deposited solder balls. Power and signals are distributed to the IC(s) by a number of lands located on conductive planes, forming carrier wiring on at least one resin fibreglass composite material layer.

Pref. each adjacent conductive plane pair is separated by one resin composite layer. The power and signal distribution wiring pref. includes interlevel vias. At leat one conductive plane may be an internal conductive plane. Each **insulating layer** may be sandwiched between a pair of conductive planes. A deposited encapsulant may be coated fro protection on the chip electrical connections to the carrier.

USE/ADVANTAGE - Surface **mount** carrier; may be **mounted** in standard DIP or PLCC package. Reduced multi-chip package cost, improved reliability and heat transfer.
Dwg.2A/4

L36 ANSWER 13 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1993-390446 [49] WPIX
DNN N1995-162349
TI Encapsulated semiconductor multichip module for integrated circuits - has wiring layers with large current capacity provided on insulating substrate together with IC chips, while wiring layers having small current capacity are formed on flexible **insulating film**.
DC U11 U14
IN ENDO, K
PA (TOKE) TOSHIBA KK
CYC 3
PI JP 05291489 A 19931105 (199349)* 6p
US 5422515 A 19950606 (199528)B 9p
KR 9612650 B1 19960923 (199926)
ADT JP 05291489 A JP 1992-94267 19920414; US 5422515 A US 1993-34868 19930319; KR 9612650 B1 KR 1993-6092 19930413
PRAI JP 1992-94267 19920414
AB US 5422515 A UPAB: 19950721 ABEQ treated as Basic
The module includes an insulating substrate (23) having power supply wiring layers (24). A number of electronic components, e.g. IC chips, are **mounted** on the substrate, via **mount** beds (25), and have **bonding pads**. An insulating sheet (28) provided above the substrate covers the electronic components and has small current wiring layers (29).

A number of apertures (30) are formed in the insulating sheet through which the power supply and small current wiring layers are electrically connected **via** bonding **wires** (33).The small current wires function as signal lines.

L36 ANSWER 14 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1992-293943 [36] WPIX
CR 1997-375146 [35]
DNN N1992-225186
TI Miniaturised electronic circuit package for space exploration - has semiconductor chips connected to bus lines provided on substrate with die

bonding ground connected through **insulating layer** by via holes.

DC T01 U11 U14 V04 W06
IN AKIYAMA, M; IHARA, H; KANEKAWA, N; KAWABATA, K; OKISHIMA, T; YAMANAKA, H
PA (HITA) HITACHI LTD; (HITB) HITACHI CHEM CO LTD; (AKIY-I) AKIYAMA M; (IHAR-I) IHARA H; (KANE-I) KANEKAWA N; (KAWA-I) KAWABATA K; (OKIS-I) OKISHIMA T; (YAMA-I) YAMANAKA H
CYC 8
PI EP 501474 A2 19920902 (199236)* EN 15p
R: DE FR GB IT NL
JP 04273470 A 19920929 (199245) 11p
CA 2061949 A 19920829 (199246)
EP 501474 A3 19930113 (199346)
US 5468992 A 19951121 (199601) 13p

AB EP 501474 A UPAB: 20010815
The electronic circuit comprises at least two semiconductor chips (101-106) which are connected to a bus line (100) and to one wiring substrate (10). The bus line includes two data bus lines, one for each side of the substrate.

The wiring substrate (10) may be a multilayer wiring substrate comprising an **insulating layer** partially formed on the surface of the substrate and a die bonding ground formed on the surface of the **insulating layer**. Wiring conductors from a wiring pad and via holes are formed in the periphery and inside of the die bonding ground with wiring conductors connected to other wiring conductors through the holes.

ADVANTAGE - Provides small, light, apparatus which has high reliability.
Dwg.1/11

L36 ANSWER 15 OF 25 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1980-M1300C [51] WPIX
TI **Bonding pad** for semiconductor device - is provided by aluminium electrode connected partly to alloy wire and to **insulation layer** for heat treatment.
DC U11
IN FUJITA, K; KOMATSU, S
PA (TOKE) TOKYO SHIBAURA DENKI KK
CYC 3
PI EP 19883 A 19801209 (198051)* EN
R: DE FR GB
EP 19883 B 19860827 (198635) EN
R: DE FR GB
DE 3071718 G 19861002 (198641)
PRAI JP 1979-63219 19790524
AB EP 19883 B UPAB: 19930902
Semiconductor device includes a semiconductor substrate (31) on which semiconductor elements (not shown) are formed. A first **insulation layer** (32) is deposited at least partly on the main surface of the semiconductor substrate, and a first alloy wire (33) contacting the semiconductor element is disposed on the first **insulation layer**.

A second **insulation layer** (34) is **mounted** , at least partly, on the first alloy wire and first **insulation layer**. A second wire (35) is, at least partially, in contact with the first alloy **wire through** openings formed in the second **insulation layer**, and also contacts the first **insulation layer**, to constitute a **bonding**

pad (35A).

L36 ANSWER 16 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 2000-357760 JAPIO
TI TAB TAPE WITH REINFORCING PLATE USED CONCURRENTLY AS HEAT SINK AND SEMICONDUCTOR DEVICE
IN SUZUKI YUKIO; OTAKA TATSUYA; OMORI TOMOO; TAKAHAGI SHIGEJI; YOSHIOKA OSAMU
PA HITACHI CABLE LTD
PI JP 2000357760 A 20001226 Heisei
AI JP1999-170757 (JP11170757 Heisei) 19990617
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To obtain a T-TAB semiconductor device, which prevents a TAB tape and a stiffner from being exfoliated in their bonding face and whose reliability is further improved.
SOLUTION: In this semiconductor device, on one face of a resin **insulating film** 1, a TAB tape 20 on which **bonding pad** parts 3 and a conductor circuit pattern 2 containing laying lead parts 20 are formed is pasted via an adhesive 5 on a stiffner 6, in which a recessed part 6a for semiconductor chip **mounting** is formed in the central part, and electrodes of the semiconductor chip 9 installed in the recessed part 6a and the **bonding pad** parts 3 are connected **through** bonding **wires** 8. A region on the side of the recessed part 6a from the **bonding pads** 3 on the TAB tape 20 is coated with a solder resist 40, so as to reduce a step to the solder resist 40 in a region in which the conductor circuit pattern exists.
COPYRIGHT: (C)2000,JPO

L36 ANSWER 17 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1999-163217 JAPIO
TI SEMICONDUCTOR DEVICE
IN HORIUCHI MICHIO; AKATA HIDEYA
PA SHINKO ELECTRIC IND CO LTD, JP (CO 416101)
PI JP 11163217 A 19990618 Heisei
AI JP1998-254178 (JP10254178 Heisei) 19980908
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 6
AB PURPOSE: TO BE SOLVED:To provide a semiconductor device which is provided with a circuit board that is reduced in manufacturing cost, improved in yield, and superior in electrical properties.
CONSTITUTION: miconductor chip 10, provided with electrode terminals arranged in an area array, is **mounted** on one surface of a circuit board 5 making its side where electrode terminals are provided facing outward, **bonding pads** 22 are provided in an area array on the one surface of the circuit board 5 except for a region on which the semiconductor chip 10 is **mounted**, and the electrode terminals and the **bonding pads** 22 are connected electrically together **through** the bonding **wires** 20 composed of conductive wire each **coated** with an **insulating film**. External connection terminals 12 provided in an area array on the other surface of the circuit board 5 are each connected electrically to the **bonding pads** 22 by conduction parts 18 which are provided to the circuit board 5 penetrating through it in its thicknesswise direction.

L36 ANSWER 18 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1999-103038 JAPIO
TI IMAGE SENSING DEVICE
IN OGINO ATSUSHI; HASHIMOTO SUSUMU; MORIMOTO DAISUKE; KASUGA SHIGETAKA; ISHII

SHIGERU
PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
PI JP 11103038 A 19990413 Heisei
AI JP1997-263148 (JP09263148 Heisei) 19970929
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 4
AB PURPOSE: TO BE SOLVED:To effectively reduce the noise, by forming a conductive layer on a main plane of an insulation circuit board, forming an **insulation layer** covering the entire surface of this conductive layer, and forming conductive wirings to cover the entire conductive layer on the top of this **insulation layer**.
CONSTITUTION: vice comprises an Al or other conductive layer 15 grounded at its terminal on the top face of an insulation board 4 **mounting** a CCD chip 2 and peripheral circuit elements 3, and Al or other conductive wirings 14 formed through an Si **oxide insulation layer** 16 on the top face of the conductive layer 15. Connection pads 13 of the wirings 14 are bonded **through** Au **wires**, etc., to terminals 12 on **bonding pads** 11 of the peripheral circuit elements 3. The conductive layer 15 at the lower faces of the wirings 14 to be signal lines protects the wirings 14 from external noises.

L36 ANSWER 19 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1997-293471 JAPIO
TI CHIP-IN-GLASS FLUORESCENT CHARACTER DISPLAY TUBE
IN FUKUSHIMA KOSHIRO
PA NEC KAGOSHIMA LTD, JP (CO 399081)
PI JP 09293471 A 19971111 Heisei
AI JP1996-105221 (JP08105221 Heisei) 19960425
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 11
AB PURPOSE: TO BE SOLVED:To reduce a strain quantity due to a thermal stress during manufacturing so as to prevent any crack by forming grooves in contact with a glass substrate right under an IC chip **mounting** portion, separating an **insulating layer** in an island manner, and connecting a connecting lead to a **bonding pad**.
CONSTITUTION: **insulating layers** 21, 22 are laminated on a glass substrate 1 having an electric supply wirings formed thereon. First and second grooves are formed with a step in contact with the glass substrate 1 right under a portion **mounting** an IC chip 9. The island-like **insulating layer** 22 is coated with an adhesive polyimide resin 4, on which the IC chip 9 is **mounted**, to be thus fixed by heating and hardening for a predetermined time. In this state, a **bonding pad** 7 on the substrate 1 is connected to a connecting lead on the IC chip 9 side **via** a bonding **wire** 8. Thereafter, electrode parts and a cover glass are assembled, to be sealed by fusing frit glass. Consequently, the **insulating layer** right under the IC chip **mounting** portion is separated in an island manner, thus reducing a strain quantity due to a thermal, stress during manufacturing, so as to prevent any crack.

L36 ANSWER 20 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1995-058269 JAPIO
TI HEAT DISSIPATING BODY AND SEMICONDUCTOR PACKAGE
IN NODA KOTA
PA IBIDEN CO LTD, JP (CO 000015)
PI JP 07058269 A 19950303 Heisei

AI JP1993-206624 (JP05206624 Heisei) 19930820
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 3
AB PURPOSE: To obtain a semiconductor package which is compact and whose heatdissipating property is excellent by a method wherein one side face of a plate material composed of a high-heat-conduction material is used as a heat dissipating region and its opposite side face is used as an electronic-component **mounting** region provided with a high-density wiring layer.
CONSTITUTION: A built-up multilayer thin-film interconnection board 2 as a heat dissipating body is formed mainly of a phosphor bronze plate 3, one face of the phosphor bronze plate 3 is used as a heat dissipating region, and a built-up layers as a high-density wiring layer is formed on the other face. In the built-up **layer**, **insulating layers** 4 and wiring patterns 5 are laminated alternately, and the wiring patterns 5 are connected by via holes 6. LSI chips 8, 9 are **mounted** on die pads 7, they are **bonded** to **bonding pads** 10 **via bonding wires** 11, and the LSI chips 8, 9 are connected to connection pads 12 via the wiring patterns 5. A base unit 15 is formed mainly of a plastic material which is easy to work, a window part 16 which exposes the heat dissipating region is formed, and a connection pad 20 on the base unit 15 is connected to the connection pad 12 by a wire 23.

L36 ANSWER 21 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1991-089539 JAPIO
TI LEAD FRAME AND SEMICONDUCTOR DEVICE USING THEREOF AND MANUFACTURE OF SEMICONDUCTOR DEVICE
IN FUKUI ATSUSHI
PA MITSUI HIGH TEC INC, JP (CO 325382)
PI JP 03089539 A 19910415 Heisei
AI JP1989-225661 (JP01225661 Heisei) 19890831
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1087, Vol. 15, No. 269, P. 33 (19910709)
AB PURPOSE: To improve the bonding property of a lead frame without deforming and deteriorating the inner lead of the frame by forming the front end of each inner lead shorter and replacing the front end section of each inner lead with a conductor pattern formed on an **insulating film**, and then, connecting them by wire bonding.
CONSTITUTION: The main body R1 of this lead frame provided with numerous inner leads 1 arranged around an area for **mounting** a semiconductor element while being separated therefrom by a predetermined distance (longer than those for ordinary lead frames) and outer leads 3 is molded. Then a front end connecting section R2 is formed by forming gold patterns which are arranged corresponding to the front ends of the leads 1 and extended toward holes opened in the above-mentined area. The main body R1 and the connecting section R2 are placed on a heat sink 7 through an insulating tape 4 and the body R1 and the section R2 are joined to each other. After joining, both ends of the gold pattern 1P of the section R2 are connected respectively to the inner leads 1 of the main body section R1 and to the **bonding pad** of the semiconductor element 5 **through wires**.

L36 ANSWER 22 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1990-068940 JAPIO
TI THIN FILM PRINTED BOARD FOR BARE CHIP
IN TAKEUCHI MASAHIKO
PA NEC CORP, JP (CO 000423)
PI JP 02068940 A 19900308 Heisei

AI JP1988-220885 (JP63220885 Heisei) 19880902
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 932, Vol. 14, No. 244, P. 162 (19900524)
AB PURPOSE: To prevent short circuit and misregistration of bonding and to prevent unnecessary contact due to bonding wire by positioning a thick **film** print **insulating** pattern to prevent contact of a bonding wire between a thick film print pad and its adjoining pad. CONSTITUTION: A bare chip 2 is **mounted** on an insulating substrate 1. A thick film printed board for a bare chip is provided with a thick film print pad 4 which is connected to the substrate 1 **through wire** bonding. In this thick film printed board, a thick **film** print **insulating** pattern 6 is located between the thick film print pad 4 and its adjoining pad 4 to prevent contact of a bonding wire 5. For example, the bare chip 2 is **mounted** on the insulating substrate 1, and when a plurality of **bonding pad** 4 at the side of the insulating substrate 1 are arranged before an electric connection circuit is formed to the **bonding pad** 4 at the side of the insulating substrate 1 from a **bonding pad** 3 at the bare chip side by using the bonding wire 5, an insulating dam 6 is provided between the **bonding pads** 4 by using **insulating** thick **film** print paste.

L36 ANSWER 23 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1988-311731 JAPIO
TI SEMICONDUCTOR DEVICE
IN KOSHIMARU SHIGERU
PA NEC CORP, JP (CO 000423)
PI JP 63311731 A 19881220 Showa
AI JP1987-147650 (JP62147650 Showa) 19870612
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 742, Vol. 13, No. 15, P. 162 (19890412)
AB PURPOSE: To prevent the occurrence of the edge touch failure of bonding wires in bonding connection by a method wherein **insulating films** are formed on parts of a scribing line in such a way as to correspond to the **bonding pad** of each chip. CONSTITUTION: A scribing line 1 is a region where an Si substrate is bared and **insulating films** 2 are formed within the scribing line region 1. The places, where these films 2 are formed, are covered corresponding to a **bonding pad** 3 which is formed on each outer peripheral part of chip regions. Semiconductor devices separated into chips are **mounted** and fixed on an island 6 and thereafter, the pads 3 of the devices and bonding electrode parts (electrodes on the side of a lead frame) 5 of a lead frame are connected to each other by bonding **through** assembly bonding **wires** 4. At this time, as the films 2 are formed at places, where are within the region 1 left on the peripheries of the chips and correspond to the pads 3, the wires 4 are wired over the films 2 without fail. That is, the wires 4 are prevented from short-circuiting with the substrate 7 as there exist the films 2 and the edge touch failure of the wires can be made to nil.

L36 ANSWER 24 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1985-167436 JAPIO
TI WIRE BONDING METHOD AND CAPILLARY USED THEREFOR
IN SATO HAJIME; MASUDA MASANORI; ONO TOSHIAKI; MEGURO MASAHIRO; KAJIWARA YUJIRO
PA HITACHI LTD, JP (CO 000510)
HITACHI YONEZAWA DENSHI KK, JP (CO 485533)
HITACHI MICRO COMPUT ENG LTD, JP (CO 470864)

PI JP 60167436 A 19850830 Showa
AI JP1984-21787 (JP59021787 Showa) 19840210
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 371, Vol. 1, No. 1, P. 152 (19860107)
AB PURPOSE: To improve the reliability of semiconductor devices by a method wherein wires are **coated** with **insulation films** while a pellet is wire-bonded to external terminals.
CONSTITUTION: The first bonding is finished by thermal compression bonding under pressure at the tip of a capillary 1 in the state that a ball 6 has been **mounted** on the **bonding pad** of the pellet after formation of the ball by fusing the tip of a wire 2 by means of an electric torch or an oxygen torch. Thereafter, the wire is transferred to the bonding part of an external terminal for the second bonding while being drawn out by pulling up the capillary 1; at that time, an **insulation film** forming material having fluidity is supplied to a fluid reservoir 4 through a fluid supply through hole 5, thereby enabling the **wire** 2 passing **through** this reservoir 4 to be easily coated. Then, connecting a controller of the supply amount of the **insulation film** forming material to the through hole 5 allows free **coat** of **insulation films** to wires of arbitrary length from the first bonding part to the second bonding part.

L36 ANSWER 25 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1984-188150 JAPIO
TI SEMICONDUCTOR DEVICE
IN OZAKI HIROSHI; OKINAGA TAKAYUKI; OTSUKA KANJI
PA HITACHI MICRO COMPUT ENG LTD, JP (CO 470864)
HITACHI LTD, JP (CO 000510)
PI JP 59188150 A 19841025 Showa
AI JP1983-60888 (JP58060888 Showa) 19830408
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 299, Vol. 9, No. 471, P. 117 (19850227)
AB PURPOSE: To **mount** a semiconductor in a high density by forming the wire bonding surface of an insulating substrate and a cap sealing surface in the same plane, thereby reducing the size of the profile of the substrate.
CONSTITUTION: A **bonding pad** of a semiconductor pellet 2 which is **mounted** by a solder material 4 of gold-silicon on a pellet **mounting** surface 5 in a cavity 3 of an insulating substrate 1 of a package is electrically connected to metallized wirings of the wire bonding surface of the substrate 1 **via** a **wire** 6. The wire bonding surface is formed in the same plane as the sealing surface of a cap 8, and the cap 8 is hermetically sealed through a low melting point glass 9 on an **insulating film** 12. Thus, a wire bonding and a cap sealing can be achieved in a narrow area, thereby reducing the size of the insulator 1.

```
     FILE 'HCAPLUS' ENTERED AT 11:34:29 ON 01 APR 2002

     FILE 'REGISTRY' ENTERED AT 11:34:58 ON 01 APR 2002
L1       134314 S W/ELS

     FILE 'HCAPLUS' ENTERED AT 11:35:18 ON 01 APR 2002
L2         1766 S (BOND?)(2N)(PAD OR PADS)
L3       219516 S (DIELETRIC  OR INSULAT? OR OXIDE)(2N)(FILM OR LAYER? OR COAT#
L4        10644 S (VIA OR THROUGH OR PATH)(2N)(LINES OR LINE OR WIRE OR WIRES O
L5       180038 S STACK### OR MOUNT? OR PILE OR PILED OR MOUND?
L6       138770 S TUNGSTEN OR WOLFRAM
L7          210 S L2 AND L5
L8       241277 S PARALLEL OR (SIDE(2N)BY(2N)SIDE) OR COLLATERAL
L9       147372 S (METAL?)(2N)(FILM OR LAYER? OR COAT#### OR MULTILAYER? OR (MU
L10          28 S L7 AND L3
L11          23 S L7 AND L9
L12           9 S L7 AND L4
L13          28 S L10 NOT L12
L14          14 S L11 NOT (L12 OR L10)
L15          16 S (L1)(L)(L4)
L16          15 S L15 NOT (L10-14)
L17          10 S L2 AND (METAL?(2N)PLATE)
L18          10 S L17 NOT (L10-16)
L19         107 S L2 AND (L6 OR L1)
L20           1 S L19 AND L4
L21          13 S L19 AND L5
L22           5 S L21 NOT (L10-18)
L23          49 S L19 AND (L9 OR (METAL?(2N)PLATE))
L24          41 S L23 NOT (L10-18 OR L21)
L25          20 S L24 AND L3
L26           2 S L7 AND L8
L27           1 S L26 NOT (L10-18 OR L21 OR L25)
```

L12 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:868927 HCAPLUS
DN 136:14107
TI Fabrication of semiconductor device with elimination or reduction of **bond pad** cracking and metal peel off
IN Liang, Zhongning; Lous, Erik Jan
PA Neth.
SO U.S. Pat. Appl. Publ., 4 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2001045669	A1	20011129	US 2001-829797	20010410
PRAI EP 2000-201315	A	20000412		

AB The invention relates to a semiconductor device comprising a **bond pad** structure, which **bond pad** structure comprises a **bond pad** disposed above .gtoreq.1 layered structure, but preferably a **stack** of layered structures, in which the layered structure comprises a metal layer and a layer of a dielec. material. In the layer of dielec. material **via lines** are present and arranged in such a way that the metal layers and the **via lines** form isolated areas filled with the dielec. material.

L12 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:253143 HCAPLUS
TI Semiconductor device and method for producing the same
IN Ozawa, Kaname; Okuda, Hayato; Nomoto, Ryuji; Akashi, Yuji; Hiraiwa, Katsuro
PA Fujitsu Limited, Japan
SO U.S., 22 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6215182	B1	20010410	US 2000-531232	20000320
PRAI JP 1999-297410	A	19991019		

AB A semiconductor device includes the first through third semiconductor devices which are **stacked** on a substrate and the first **through** third **wires** for connecting the semiconductor elements and the substrate. The first wires serve to connect electrodes of the first semiconductor element positioned uppermost and electrodes of the second semiconductor element. The second wires serve to connect the electrodes of the second semiconductor element and electrodes of the third semiconductor element. The third wires serve to connect the electrodes of the third semiconductor element and **bonding pads** of the substrate. Between the first wires and the electrodes of the second semiconductor element and between the second wires and the electrodes of the third semiconductor element, stud bumps are provided so as to form space therebetween, thereby avoiding short-circuits therebetween.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:131180 HCAPLUS
DN 134:156520
TI Improving copper pad adhesion in fabricating an integrated circuit
IN Chen, Sheng-hsiung
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6191023	B1	20010220	US 1999-442497	19991118
	US 2001016415	A1	20010823	US 2001-755282	20010108
PRAI	US 1999-442497	A3	19991118		

AB This invention relates to a new improved method and structure in the fabricating of Al metal pads. The formation special Al **bond pad** metal structures are described which improve adhesion between the Ta nitride pad barrier layer and the underlying Cu pad metallurgy by a special interlocking **bond pad** structure. It is the object of the present invention to provide a process wherein a special **grid** of interlocking **via** structures is placed in between the underlying Cu pad metal and the top Ta nitride pad barrier layer providing improved adhesion to the Al pad metal **stack** structure. This unique contact **bond pad** structure provides for thermal stress relief, improved wire bond adhesion to the Al pad, and prevents peeling during wire bond adhesion tests.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:906048 HCAPLUS
TI Semiconductor device with reduced thickness
IN Inaba, Takehito; Ichinose, Michihiko; Oyachi, Kenji
PA Nec Corporation, Japan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6166443	A	20001226	US 1999-300683	19990427
	TW 407365	B	20001001	TW 1999-88106995	19990429
PRAI	JP 1998-121046	A	19980430		

AB Internal electrodes and external lead wiring lines are formed on the front surface of a substrate of a semiconductor device, and solder bumps electrically connected to the external lead wiring **lines** **via through** holes are provided on the rear surface of the substrate. A first semiconductor chip is **mounted** on the surface of the substrate, and a second semiconductor chip is **mounted** on the rear surface of the substrate. Electrodes of the first semiconductor chip are connected to **bonding pads** at one side ends of the internal wiring lines, and electrodes of the second semiconductor chip are connected to the **bonding pads** at the other ends of the internal wiring lines and the external lead wiring lines with bonding **wires** passing **through** openings provided in the substrate. The solder bumps are formed with a height equal to or greater than the thickness of the second

semiconductor chip so that, when the semiconductor device is **mounted** on an external **mounting** board or the like, a gap is formed between the substrate of the semiconductor device and the external **mounting** board by the height of the solder bumps themselves. The second semiconductor chip **mounted** on the rear surface of the substrate is accommodated in the gap.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:902089 HCAPLUS
DN 134:186564
TI Multiple through-wafer interconnects for **stacking** of microsystems
AU Heschel, Matthias; Rasmussen, Kurt; Kuhmann, Jochen F.; Bouwstra, Siebe
CS Mikroelektronik Centret, DTU, Lyngby, DK-2800, Den.
SO Micro-Electro-Mechanical Systems (1999), 1, 537-540
CODEN: MSIYAW
PB American Society of Mechanical Engineers
DT Journal
LA English
AB This paper describes a novel technol. for multiple wafer front-side to backside interconnects, which was applied to a multifunctional interconnect layer for an integrated microphone for hearing aid applications. Besides the interconnect layer with relatively large through-holes the **stack** consists of the microphone itself and an integrated circuit chip for signal conditioning. The patterning of the metalization on the interconnect wafer was done using electrodepositable photoresist as mold for electroplating of a variety of metals. For the interconnect metalization the authors use copper. The **bonding pads** on the microphone side of the interconnect layer were provided with under bump metalization (UBM) and solder bumps. The IC side features a top surface metalization (TSM) suitable for conductive adhesive bonding. The realized feed-**through wires** show good elec. performance in terms of low series resistance (100 m.OMEGA.) and small parasitic capacitance (< 1 pF).

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:582782 HCAPLUS
TI Flip-chip interconnection having enhanced electrical connections
IN Takano, Eiji; Shimizu, Shinya
PA Kabushiki Kaisha Toshiba, Japan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5952727	A	19990914	US 1997-819935	19970318
PRAI JP 1996-62847		19960319		

AB One-side ends of fine metal wires are **bonded** onto **pads** of a semiconductor chip **via wire** bonding and the other ends of the fine metal wires are **mounted** on the board by flip chip.

L12 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS

AN 1996:546532 HCAPLUS
DN 125:236210
TI Process and apparatus for manufacturing integrated circuits using an automated multistation apparatus including an adhesive dispenser
IN Takahashi, Tetsuo; Miyauchi, Eisaku; Mogi, Kunio; Araya, Shinichi
PA Tdk Corporation, Japan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5549716	A	19960827	US 1993-46151	19930413

AB A process and app. for manufg. an electronic component capable of permitting die-bonding, wire-bonding, and molding to be successively executed on a **through-line** are described. Die-bonding for adhesively **mounting** IC chips on a lead frame, wire-bonding for connecting **bonding pads** of the IC chips and the lead frame to each other **through** lead **wires**, and molding for forming a resin material into an outer package for covering each of the IC chips are successively executed on a **through-line** while transferring the lead frame by means of a conveyor. The app. includes automatic inspection means.

L12 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:93378 HCAPLUS
DN 120:93378
TI Plasma-polymerized coatings for electrical connectors
IN Benz, Gerhard; Doerfler, Reiner; Mayer, Hans
PA Bosch, Robert, G.m.b.H., Germany
SO PCT Int. Appl., 12 pp.
CODEN: PIXXD2
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9317049	A1	19930902	WO 1993-DE97	19930205
W: JP, US				
RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
PRAI DE 1992-9202251		19920221		
DE 1992-9206834		19920520		

AB Supports, esp. metal supports, connectors, or circuit boards provided with .gtoreq.1 semiconductor chip (e.g., a Si pressure sensor) which is connected to .gtoreq.1 **bonding pad via bonding wires** are described in which the exposed surfaces of the chip, wires, and **bonding pads** are coated with an org. protective layer produced by plasma polymn. The protected systems may be **mounted** in automobile wheels.

L12 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:506016 HCAPLUS
DN 119:106016
TI IR image sensor apparatus cooled by Dewar vessel
IN Ono, Katsuhiro; Wada, Akifumi; Sugiura, Yasusuke; Yasunaga, Masatoshi
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF

DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04364778	A2	19921217	JP 1991-168926	19910611
	JP 3075777	B2	20000814		

AB The title app. comprises: an IR sensor array **mounted** on a subpackage; a ceramic circuit board disposed in the same plane as the subpackage; and a Dewer vessel for housing the IR sensor array, wherein the **bonding pads** of the subpackage and the circuit board are elec. connected **through** a **wire** bonding.

L13 ANSWER 1 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:116261 HCAPLUS
DN 136:143921
TI **Stacked** package with shortened signal paths
IN Baek, Hyung Gil
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
KR 2000027503	A	20000515	KR 1998-45448	19981028

AB A **stacked** package is provided to shorten signal transfer paths by connecting a lead frame to a pad through a pattern film, thereby preventing delay in signal transfer. A **stacked** package comprises upper and lower semiconductor chips, a lead frame, sealing material and solder balls. The lead frame is bonded on a rear surface of the chips. A pattern film longer than a conductive base is bonded on an inner surface of the base. Metal films are attached on both sides of an **insulation film**. Via holes are formed on the pattern film for connecting the metal films. The inner wall of the metal films is coated with conductive metal. The pattern film is **bonded** on **pads** of the chips. The portion between both bases is molded with the sealing material. The solder balls are attached to the bottom of the base.

L13 ANSWER 2 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:26369 HCAPLUS
TI Integrated circuits packaging system and method
IN Brown, Sammy K.; Avery, George E.; Wiggin, Andrew K.; Beal, Samuel W.
PA Alpine Microsystems, Llc, USA
SO PCT Int. Appl.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2002003422	A2	20020110	WO 2001-US20727	20010629
W: CN, JP, SG				
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
PRAI US 2000-608446	A	20000629		

AB A plurality of integrated circuits are efficiently interconnected to improve the electrical performance of the overall system. This is accomplished by providing high speed, high density, system level interconnect, including interchip routing lines, on the integrated circuit devices, thereby reducing the routing complexity of the substrate or board. The devices are **mounted** directly on the board. An integrated circuit device comprises an integrated circuit region including integrated circuit elements. An interconnect **layer** includes an **insulative** material, a plurality of conductive traces, and a plurality of conductive **bond pads** arranged in first and second subsets. A first subgroup of the conductive traces are connected to the integrated circuit elements in the integrated circuit

region and are connected to the first subset of conductive **bond pads**. A second subgroup of the conductive traces are electrically insulated from the integrated circuit elements and are electrically insulated from the first subgroup of the conductive traces to form a pass through. The second subgroup of the conductive traces are connected to the second subset of conductive **bond pads**.

L13 ANSWER 3 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:836259 HCAPLUS
DN 135:351501
TI Method for making DRAM having a brush-type **stacked** capacitor using a HSG mask
IN Chen, Li-Ye
PA Vanguard International Semiconductor Corp., Taiwan
SO Taiwan, 33 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
TW 382812	B	20000221	TW 1998-87111341	19980713

AB A method for making a DRAM having a brush-type **stacked** capacitor by a hemispherical grain (HSG) mask comprises: forming a field **oxide layer** on a semiconductor substrate with device region for the manuf. of semiconductor devices; forming said semiconductor device structure in the device region of said semiconductor substrate; depositing a first **insulation layer** on said device region and said field oxide region; applying a planarization treatment on said first **insulation layer**; forming a first opening going through said device region on said first **insulation layer** so that said contact opening can be used to form a **stacked** capacitor array; depositing a first polysilicon layer on said first **insulation layer** and filling said first opening; depositing a first metal silicide on said first polysilicon layer to form a polycide layer; using a mask and a selective anisotropic plasma etching to define said polysilicon metal layer until said first **insulation layer** to form bit lines and leaving a portion of said polysilicon layer on said first opening as the contact of said **stacked** capacitor and a **bonding pad**; depositing a second **insulation layer** on said bitlines and said first polysilicon in said first opening.

L13 ANSWER 4 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:392126 HCAPLUS
DN 134:375090
TI Package with high bending and breaking strength having very thin semiconductor chip, multichip module assembled by the package, and method for manufacturing the same
IN Asada, Junichi
PA Kabushiki Kaisha Toshiba, Japan
SO U.S., 27 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6239496	B1	20010529	US 2000-484032	20000118

	US 2001012643	A1	20010809	US 2001-828131	20010409
PRAI	JP 1999-9763	A	19990118		
	US 2000-484032	A3	20000118		

AB A semiconductor package of this invention has an **insulating** substrates, wiring **layers** disposed on the surface of the insulating substrate, a semiconductor chip disposed in a device hole provided in the insulating substrate, inner-joint-conductors for connecting at least part of the **bonding pads** on the surface of the semiconductor chip to the corresponding inner-joint-conductors and connection lands connected to the wiring layers. The device hole is provided so that it goes through the center of the insulating substrate. The semiconductor chip is thinner than the insulating substrate. Then, this semiconductor chip is disposed in the device hole such that a bottom thereof is flush with a bottom plane of the insulating substrate. Further, this invention provides a MCM in which plural pieces of the thin semiconductor packages are laminated. In the MCM, the semiconductor packages are laminated such that top and bottom faces of the thin Si chip are inverted. Predetd. connection lands are elec. connected to each other through a connecting conductor. This MCM has a high mech. strength in its **stacked** structure and there is a low possibility that crack may occur in the package due to stress in the bending direction.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 5 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:294834 HCAPLUS
DN 134:289061
TI Flip chip **mounting** technique
IN Estes, Richard H.; Ito, Koji; Akita, Masanori; Mori, Toshihiro
PA Polymer Flip Chip Corp., USA; Toray Engineering Co.
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6219911	B1	20010424	US 1999-274748	19990323
	US 6189208	B1	20010220	US 1999-378847	19990823
PRAI	JP 1998-95463	A	19980323		
	US 1999-274748	A2	19990323		

AB In a flip chip bonding method, polymer bumps are formed, using a bonding tool, on an IC chip, held via suction to the bonding tool. An **insulating** adhesive **film** is pressed onto the upper surface of a circuit board held via suction with a suction stage. Heat is then applied to bring the film into close contact with **bond pads** of the circuit board. At this point, the bonding tool is moved downward, bonding the polymer bumps to the circuit board electrodes. During the time of this downward movement, bonding of the polymer bumps to the circuit board **bond pads** can be achieved by piercing the **insulating** adhesive **film** with the polymer bumps, and strong bonding can be achieved with adequate reliability. This method eliminates the need for a process in which through-holes must be pierced in the **insulating** adhesive **film** to accommodate the polymer bumps.

RE.CNT 63 THERE ARE 63 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 6-28

L13 ANSWER 6 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:278058 HCAPLUS
DN 134:274568
TI Mold-BGA-type semiconductor device and method for making the same
IN Kimura, Naoto
PA NEC Corporation, Japan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6218728	B1	20010417	US 1998-179154	19981026
PRAI JP 1997-295305	A	19971028		

AB Disclosed is a mold-BGA-type semiconductor device which has: a semiconductor chip which includes **insulating** resin **film** formed on at least a part of the surface of the semiconductor chip except a pad; a conductive layer formed in a region on the **insulating** resin **film**, the region including at least part corresponding to a position where a solder ball is **mounted**; a 1st metal thin wire which is wire-**bonded** between the **pad** and the conductive layer; a 2nd metal thin wire which is wire-bonded on the conductive layer; resin part which seals the semiconductor chip, the resin part including a hole to expose part of the 2nd metal thin wire; and a solder ball which is **mounted** on the hole.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 7 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:131247 HCAPLUS
DN 134:156532
TI Semiconductor chip carrier having partially buried conductive pattern and semiconductor device using the same
IN Senba, Naoji; Takahashi, Nobuaki
PA NEC Corporation, Japan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6191482	B1	20010220	US 1998-62657	19980420
PRAI JP 1997-103089	A	19970421		

AB A semiconductor chip is **mounted** on a semiconductor chip carrier through a flip chip bonding technique; the semiconductor chip carrier includes an **insulating layer** such as synthetic resin having a **mounting** area assigned to the semiconductor chip and a conductive pattern having **pads bonded** to bumps of the semiconductor chip, and only the pads are formed in the **mounting** area so that melted synthetic resin smoothly flows into the gaps between the **insulating** synthetic resin **layer** and the semiconductor chip.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 8 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:129818 HCAPLUS
DN 134:171823
TI Flip chip **mounting** technique using conducting polymers for electrically connecting electronic packages to substrates
IN Estes, Richard H.; Ito, Koji; Akita, Masanori; Mori, Toshihiro; Wada, Minoru
PA Polymer Flip Chip Corp., USA; Toray Engineering Co.
SO U.S., 12 pp., Cont.-in-part of U. S. Ser. No.274,748.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6189208	B1	20010220	US 1999-378847	19990823
	US 6219911	B1	20010424	US 1999-274748	19990323
PRAI	US 1999-274748	A2	19990323		
	JP 1998-95463	A	19980323		

AB The invention provides a flip chip **mounting** process in which a **layer** of elec. **insulating** adhesive paste is applied on a substrate having **bond pads**, covering the **bond pads** with the adhesive. Elec. conductive polymer bumps are formed on **bond pads** of a flip chip to be bonded to the substrate, and the polymer bumps are at least partially hardened. The **bond pads** of the flip chip are then aligned with the **bond pads** of the substrate, and the at least partially hardened polymer bumps are pushed through the adhesive on the substrate to contact directly and bond the polymer bumps to the **bond pads** of the substrate. This process results in direct elec. and mech. bonding of the polymer bumps between the chip and substrate **bond pads**, even though the adhesive film was applied on the substrate in a manner that covered the substrate **bond pads**. The polymer bumps displace the adhesive as they are pushed through it and expand laterally on the substrate **bond pads**. As a result, the area around the polymer bumps between the chip and the substrate is filled with the adhesive, in the manner of an underfill, whereby a sep., post-bond underfill process is not required.
RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 9 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:57261 HCAPLUS
DN 134:124639
TI SiO2 wire bond insulation in semiconductor assemblies
IN Manteghi, Kamran
PA Philips Electronics North America Corporation, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6177726	B1	20010123	US 1999-249227	19990211

AB A semiconductor integrated circuit package is provided with insulated bonding wires. The semiconductor die is **mounted** to a base of either a leadframe or a grid-array package. A plurality of bonding wires

are **bonded** between **bonding pads** on the semiconductor die and bonding fingers at inner ends of package conductors. The bonding wires have a PECVD SiO2 layer formed thereupon to thereby provide elec.-insulated bonding wires to prevent short-circuits between adjacent bonding wires. After wire bonding of the bonding wires, an **insulating** PECVD SiO2 **layer** is formed on the bonding wires to prevent short-circuits with adjacent wires. An SiO2 layer is simultaneously formed on a leadframe and is removed from the outer ends of the leads by blasting with a medium.

RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 10 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:891604 HCAPLUS
DN 134:50171
TI Semiconductor device having pads for connecting a semiconducting element to a mother board
IN Oohira, Minoru; Ohgiyama, Kenji; Fujihara, Teruhisa
PA Mitsubishi Denki Kabushiki Kaisha, Japan
SO U.S., 25 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6163069	A	20001219	US 1998-70724	19980501
PRAI JP 1997-277230	A	19971009		

AB A discrete semiconductor device and method are provided for small signal operation with a smaller packaging area. The device has excellent high frequency characteristics and good heat dissipation performance. The discrete semiconductor elements are **mounted** on die **bond pads** and wire **bond pads**, with the packaging surface being sealed with a resin and connecting the back faces of the die **bond pads** and the wire **bond pads** directly to a mother board.

RE.CNT 27 THERE ARE 27 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 11 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:830375 HCAPLUS
DN 133:368491
TI Method of using a silicon oxynitride anti-reflective coating for final metal layer
IN Shields, Jeffrey A.; Rangarajan, Bharath
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6153504	A	20001128	US 1999-375004	19990816

AB A SiON anti-reflective coating (ARC) is formed on the uppermost metal or **bonding pad** layer, a topside protective **layer**, e.g., **oxide**, nitride or oxynitride, formed thereon and etching is conducted through the topside protective layer and SiON ARC to form a **bonding pad** opening. The use of SiON as an ARC reduces

1st semiconductor chip includes a 1st face in which a **bonding pad** disposed, and a 2nd face opposite to the 1st face. A 1st **insulating layer** is **coated** over the 1st face of the 1st semiconductor chip so as to expose the **bonding pad**. A metal pattern is deposited on the 1st **insulating layer** and one end of the metal pattern is connected to the exposed **bonding pad**. A 2nd **insulating layer** having a via hole exposing the metal pattern and a ball land, is coated over the 1st face of the 1st semiconductor chip. A 2nd semiconductor chip includes a 1st face in which a **bonding pad** is disposed and opposite to the 1st face of the 1st semiconductor chip, and a 2nd face opposite to the 1st face of the 2nd semiconductor chip. The 2nd semiconductor chip is opposed from the 1st face of the 1st semiconductor chip by a selected distance. A 3rd **insulating layer** is **coated** on the 1st face of the 2nd semiconductor chip so as to expose the **bonding pad** of the 2nd semiconductor chip. A conductive bump is formed at the **bonding pad** of the 2nd semiconductor chip. The conductive bump is inserted into the via hole, thereby elec. connecting the 1st and the 2nd semiconductor chips with a medium of the metal pattern. A solder ball is **mounted** in the ball land, and the solder ball is formed with a size that is large enough to be protruded from the 2nd face of the 2nd semiconductor layer.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 14 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:157671 HCAPLUS
DN 132:174566
TI SiO2 wire bond insulation in integrated circuit packaging
IN Manteghi, Kamran
PA VLSI Technology, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6033937	A	20000307	US 1997-996836	19971223

AB An integrated circuit package is provided with insulated bonding wires. The semiconductor die is **mounted** to a base of either a lead frame or a grid-array package. A plurality of bonding wires are **bonded** between **bonding pads** on the semiconductor die and bonding fingers at inner ends of package conductors. The bonding wires have a PECVD SiO2 layer to provide elec. insulated bonding wires to prevent short circuits between adjacent bonding wires. After wire bonding of the bonding wires, an **insulating** PECVD SiO2 **layer** is formed on the bonding wires to prevent short circuits with adjacent wires. A SiO2 layer is simultaneously formed on a lead frame and is removed from the outer ends of the leads by blasting with a medium.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L13 ANSWER 15 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:670618 HCAPLUS
DN 131:340301
TI Intermetallic growth and void formation in Au wire ball **bonds** to Al **pads**

AU Uno, Tomohiro; Tatsumi, Kohei
CS Advanced Technology Research Laboratories, Nippon Steel Corporation, Kawasaki, 211-0035, Japan
SO Nippon Kinzoku Gakkaishi (1999), 63(7), 828-837
CODEN: NIKGAV; ISSN: 0021-4876
PB Nippon Kinzoku Gakkai
DT Journal
LA Japanese
AB To clarify the reliability of Au wire **bonds** to Al **pads**, void formation and diffusion were investigated using bonds annealed at various temps.(423-573 K). We investigated the effects of the annealing environments, Al **pad** thickness, and **bonding** conditions on void formation. Voids became larger only when Au-Al intermetallics grew non-uniformly, whereas deleterious voids were not obsd. in the bonds annealed in vacuum. An **oxide film** on the surface of Al pads acts as a diffusion barrier at the interface. Optimized bonding conditions (applied pressure, ultrasonic energy) broke up the **oxide film**, resulting in redn. of void formation. Au5Al2 phase grew dominantly in the early stage of diffusion, then it transformed into Au4Al phase because the Al layer was completely consumed. The activation energy Q of transmission velocity at the Au/Au4Al boundary was 0.85 eV (82 kJ/mol). This is similar to the activation energy of the bond failure by annealing. These results indicate that void formation has a great correlation with the Au4Al growth. It is predicted that the non-uniform diffusion behavior causes vacancies to **pile**-up and these vacancies coalesce to form several types of voids in the interface.

L13 ANSWER 16 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:545498 HCAPLUS
DN 131:178307
TI Multilayer printed circuit boards for **mounting bonding pads**
IN Kume, Kenshi
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11233679	A2	19990827	JP 1998-35105	19980217

PI JP 11233679 A2 19990827 JP 1998-35105 19980217
AB The title circuit boards comprise (1) a substrate, (2) thin-film circuit layers each formed over through holes on an org. polymer **insulator layer** and laminated to give a multilayer circuits provided on the substrate, and (3) **bonding pads** provided on the top circuit layer for **mounting** semiconductor chips and/or elec. components, wherein the **bonding pads** are formed on the bottom of the through holes on the top circuit layer. The employment of thin-film circuit layers and formation of **bonding pads** in through holes gives the circuit boards high integration and **mounting** on the **bonding pads** security.

L13 ANSWER 17 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:468117 HCAPLUS
DN 131:96125
TI Compound semiconductor device with a stripe-shaped heterojunction bipolar transistor cell region **mounted** on a semi-insulating semiconductor substrate

IN Asano, Tetsuro
PA Sanyo Electric Co., Ltd., Japan
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5929468	A	19990727	US 1997-959299	19971028
	JP 10135236	A2	19980522	JP 1996-290714	19961031
	JP 10135237	A2	19980522	JP 1996-290715	19961031
PRAI	JP 1996-290714		19961031		
	JP 1996-290715		19961031		

AB A compd. semiconductor device has a stripe-shaped heterojunction bipolar transistor cell region **mounted** on a semi-insulating semiconductor substrate and comprising an array of unit transistor cells each having a base region, an emitter region, and a collector region. A base wiring electrode and a collector wiring electrode are disposed on the substrate parallel to the cell region. The base wiring electrode and the collector wiring electrode have toothed shapes connected to the base region and the collector region. A heat-radiating electrode is disposed on the substrate parallel to the cell region with the base wiring electrode or the collector wiring electrode. A relatively thick Au-plated layer is connected to the heat-radiating electrode and the emitter regions of the unit cells and has a bridge structure over the base wiring electrode or the collector wiring electrode with an **insulating film** interposed there between. First and 2nd **bonding pads** are disposed on the substrate near one and opposite sides thereof and connected to the base wiring electrode and the collector wiring electrode, resp.

L13 ANSWER 18 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:425714 HCAPLUS
DN 131:52767
TI Forming **bond pads** in integrated circuits by dual damascene etching
IN Schnabel, Rainer Florian; Ning, Xian J.; Spuler, Bruno
PA Siemens Aktiengesellschaft, Germany
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 926721	A2	19990630	EP 1998-120465	19981029
	EP 926721	A3	20011219		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6033984	A	20000307	US 1997-997682	19971223
	TW 436930	B	20010528	TW 1998-87118611	19981109
	CN 1223461	A	19990721	CN 1998-123100	19981221
	JP 11312704	A2	19991109	JP 1998-365074	19981222
PRAI	US 1997-997682	A	19971223		

AB An improved method of forming a **bond pad** by performing a dual damascene etch through a layer **stack** disposed above a substrate using self-aligned vias is described. The layer **stack** includes an underlying conductive **layer** and an

insulating layer disposed above the underlying conductive layer. At least 1 via hole is formed in the **insulating layer** positioned over the underlying device layer and extending to the underlying device layer. A **bond pad** trench is then formed that takes the form of the desired **bond pad** . A layer of conductive material is then placed over the **insulating layer**, substantially simultaneously filling the via hole and the **bond pad** trench. The **bond pad** is then formed by removing the layer of conductive material sufficiently to expose the upper surface of the **insulating layer**.

L13 ANSWER 19 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:343535 HCAPLUS
DN 130:345900
TI Electronic printed circuit boards and fabrication thereof by polymer sealing
IN Morofuji, Takeshi; Unoki, Shigesachi
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11145180	A2	19990528	JP 1997-313259	19971114

AB The title fabrication involves (1) forming a metal circuit layer on a substrate, (2) covering the circuit layer with a glass **insulator layer** which has an opening over a metallic die **pad** and a **bonding** connecting contact to be surrounded by the sidewall of the glass layer, (3) **mounting** a semiconductor chip on the die pad, (4) connecting the chip and the bonding connecting contact with a bonding wire, (5) sealing the chip, the bonding wire, and the bonding connecting contact with a polymer, (6) printing a solder layer on a **mounting** pad which is connected by the circuit layer outside the opening, and (7) subsequently **mounting** another chip on the solder-printed layer. The sealing of the chip, the bonding wire, and the bonding contact with a polymer sealant gives the circuit boards an improved reliability and the glass opening prevents excess flowing of the polymer sealant outside the area.

L13 ANSWER 20 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:816427 HCAPLUS
DN 130:103700
TI Multilayer printed circuit boards
IN Baniwa, Hideaki
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10341082	A2	19981222	JP 1997-152262	19970610

AB The circuit boards contain substrates, alternately laminated org. resin layers and interconnection conductor layers, through hole conductors in resin layers for elec. connecting upper and lower conductor layers,

bonding pads elec. connected with the top conductor layers and **mounting** electronic parts, and subsidiary org. resin layers around the conductor layers. The electrodes of the electronic parts are firmly elec. connected to certain conductor layers.

L13 ANSWER 21 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:816398 HCAPLUS
DN 130:89283
TI Fabrication of semiconductor device with aluminum pads suitable for wire bonding
IN Hoshino, Kazuhiro
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10340920	A2	19981222	JP 1997-151749	19970610

AB A semiconductor chip is used which has a wiring on the upper surface of a substrate, an **insulating film** covering the wiring, and holes formed in the **insulating film**. A film consisting of an Al-contg. conductive material is selectively formed, esp., by CVD, in the holes to obtain pads. The chip is **mounted** on a substrate, and the **pads** are wire **bonded** to the conductive portions on the substrate. The device has high elec. reliability.

L13 ANSWER 22 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:599518 HCAPLUS
DN 129:268848
TI Multilayer circuit boards
IN Kume, Kenji
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10242650	A2	19980911	JP 1997-43676	19970227

AB Org. interlayer **insulator films** in the circuit boards contain fillers the surface of which is treated with silane-coupling agents. The circuit boards do not cause cracks in electronic parts **mounted** on **bonding pads**.

L13 ANSWER 23 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:744062 HCAPLUS
DN 128:9431
TI Crack stop formation in integrated circuit chip manufacture
IN Mitwalsky, Alexander; Ryan, James Gardner
PA International Business Machines Corp., USA; Siemens A.-G.
SO Eur. Pat. Appl., 4 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 806795	A2	19971112	EP 1997-303018	19970502
	EP 806795	A3	19971126		
	R: DE, FR, GB				
	US 5776826	A	19980707	US 1996-642983	19960506
	JP 10041255	A2	19980213	JP 1997-107014	19970424
	JP 3204158	B2	20010904		
PRAI	US 1996-642983	A	19960506		

AB A simplified crack stop formation compatible with shallow fuse etch processes which are used for modern low-cost redundancy designs using upper-level metal fuses is described. A modified last level metalization (LLM) etch according to the invention allows a high-productivity single-step **bond pad**/fuse/crack stop etch. The **stack** of metal films formed at the edge of the dicing channel is readily removed with a modified LLM etch prior to dicing, causing the **insulator films** covering the dicing channel to be phys. sepd. from the **insulators coating** the elec. active chip areas. The sepn. prevents cracks that could propagate through the insulators of the dicing channel into the active chip.

L13 ANSWER 24 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:568295 HCAPLUS
DN 121:168295
TI Integrated circuit **mounting**
PA Texas Instruments Inc., USA
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06069272	A2	19940311	JP 1993-103297	19930428
PRAI	US 1992-877967		19920430		

AB A die is used which comprises a field oxide formed on Si, a 1st barrier metal layer formed on a selected area of the field **oxide film**, an Al **bonding pad** formed on the metal layer, a 2nd barrier metal layer formed on the Al **bonding pad**, and a 2nd Au **bonding pad** formed on the 2nd barrier metal layer. The process is also claimed.

L13 ANSWER 25 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1989:86902 HCAPLUS
DN 110:86902
TI Preparation of semiconductor devices with humidity-resistance
IN Ogawa, Kichiji
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63216352	A2	19880908	JP 1987-50615	19870304

AB A semiconductor chip is **mounted** on a lead frame, Al pads on the chip are wire-bonded with leads, and then bare parts of the Al pads are coated with Al2O3 layers by dry oxidn. to give a humidity-resistant

semiconductor device. A semiconductor chip bearing a phosphosilicate glass (PSG) passivation layer was **mounted** on a lead frame, Al pads on the chip surface were wire-bonded with leads, and the bare parts of the Al pads were oxidized by UV irradn. at 350.degree. in O3 to form a thick **oxide layer** and give a highly humidity-resistant semiconductor device, while no damage was caused to the PSG layer.

L13 ANSWER 26 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1972:29092 HCAPLUS
DN 76:29092
TI Insulated-gate field-effect transistors
IN Das, Mukunda Behari; Josephy, Richard D.
PA Associated Semiconductor Manufacturers Ltd.
SO Brit., 11 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
GB 1254301		19711117	GB	19680311

AB IGFETs suitable for high-frequency, high-power operation are described. Preferably, the transistor is an n-channel, p-substrate Si IGFET, the 1st **insulating layer** being Si **oxide** and the 2nd being Si3N4. E.g., a large-area high-resistivity p-type Si slice is prepd. with 1 major surface optically flat. An **insulating layer** of Si **oxide**, 0.6 .mu. thick, is grown on the Si surface by thermal oxidn. in wet O at an elevated temp. Openings are made in the **oxide layer** and P is diffused into the surface portions of the exposed Si body. The **oxide layer** and any P glass formed during diffusion are removed from the entire surface. A drive-in step is then performed by heating the body to form n+-type source and drain regions. A fresh **oxide layer**, 0.1 .mu. thick, is thermally grown over the entire surface. Then a layer of Si3N4, 0.1 .mu. thick, is deposited on the **oxide layer** by heating the body at 850.degree. in a gas flow of SiH4 and NH3. Openings are then made in the **oxide** and nitride **layers** to expose the source and drain regions. Al is then deposited over the entire surface. The Al layer is situated on the surface of the Si3N4 layer and on parts of the source and drain regions exposed by the openings in both nitride and **oxide layers**. Photomasking and etching are carried out to define source, drain, and gate electrodes in the Al layer. The body is divided into a no. of individual transistor units. The unit is **mounted** on the header part of an envelope and connection wires are thermocompression bonded to the large **bonding pads** of the Al source, drain, and gate electrodes. Finally, the device is encapsulated.

L13 ANSWER 27 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1971:502902 HCAPLUS
DN 75:102902
TI Transistor having emitter, base, and collector regions.
IN Kerr, John A.; Wadham, Eric
PA U. S. Philips Corp.
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3595716	A	19710727	US 1968-732626	19680528
PRAI	GB 1968-24762		19680516		

AB A method is described for manufg. semiconductor devices comprising a transistor with emitter, base, and collector regions. In one example, the starting material is a slice of Si having an n+-type substrate and an n-type epitaxial layer. A **layer** of Si **oxide** is grown on the epitaxial layer by heating at 1000.degree. in wt O for 45 min. An opening is made in the **oxide layer** exposing the n-type layer. P is diffused into the exposed portion to form an n+-region adjacent the surface where the P concn. is 1-5 .times. 1020/cm3. During diffusion a layer of phosphosilicate glass is formed on the exposed Si and on the **oxide layer**. The glass and **oxide layers** are removed in the areas to be occupied by the transistor base regions. A Si **oxide layer** is deposited and densified by heating at 850.degree.. A layer of Al is vapor deposited on the **oxide layer** and then a window is formed in the Al layer over the previously formed n+-type region. B ions are then implanted into the exposed surface area. B ion implantation occurs through the **oxide layer** and the previously diffused P concn. in the n+-region. During low-temp. annealing, a base region and the locations of the emitter/base junction and collector/base junction are detd. The Al masking is removed and the body annealed at 600-800.degree. for 30 min in dry N. Further openings are formed in the oxide to expose the emitter and base regions where they extend to the surface. A layer of Al is deposited on the surface and then selectively removed to leave an emitter contact layer in the form of a finger which extends over the **oxide layer** and terminates in a **bonding pad** above the collector region, and a base contact layer in the form of 2 fingers which extend over the **oxide layer** and terminates in a **bonding pad** above the collector region. The slice is divided into units which are individually **mounted** on a header and appropriate connections made.

L13 ANSWER 28 OF 28 HCAPLUS COPYRIGHT 2002 ACS
AN 1971:412304 HCAPLUS
DN 75:12304
TI Semiconductor devices
IN Kerr, John A.; Wadham, Eric
PA Associated Semiconductor Manufacturers, Ltd.
SO Brit., 13 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1228754		19710421	GB	19670526

AB Methods are described for the manuf. of semiconductor devices, e.g., a semiconductor device consisting of a discrete transistor, or a semiconductor integrated circuit including a transistor. In one example, the starting material is an n+ type Si substrate having an n-type epitaxial layer on it. A **layer** of Si **oxide**, 3000 .ANG. thick, is grown on the epitaxial layer surface. An opening 25 .times. 30 .mu., is formed in the thermally grown **oxide layer**. A thinner **layer** of Si **oxide** (1000 .ANG.) is grown on the exposed part of the body. A layer of Al (1 .mu.) is evapd. over the whole surface of the **oxide layers**.

An opening, 3 .times. 20 .mu., is formed in the Al layer exposing the underlying thin portion of the **oxide layer**. This opening is centrally disposed within the area occupied by the thin **oxide layer**. The body is placed in the target chamber of an ion implantation app. and implantation of P ions is effected into the body in the area exposed by the opening in the Al layer. The implantation energy is 80 kW, the dose is 1016/cm2, and the orientation of the body is such that there is an angle of 7.degree. between the ion beam axis and the (111) direction. The Al mask is removed and the body annealed in dry N at 900.degree. for 30 min. After annealing the P surface concn. in the implanted n+ type region is .apprx.1020/cm3. The latter procedure is repeated with the implantation of B ions in the exposed area. Implantation of B ions occurs through the Si **oxide layer** and through the previously implanted P concn. in the n+ region. During annealing at a relatively low temp., a base region and the locations of an emitter/base junction and a collector/base junction are simultaneously detd. Subsequent to the B ion implantation the residual Al layer is removed and the body annealed in dry N at 600-800.degree. for 30 min. After annealing the B surface concn. in the base region is .apprx.1018/cm3. The emitter/base junction is situated at a depth from the surface of 0.25 .mu. and the collector/base junction at a depth of 0.4-0.5 .mu., giving a base region width of 0.15-0.25 .mu.. Openings are formed in the Si **oxide layer** portion to expose the emitter and the base regions where they extend to the surface. The opening exposing the emitter region is 1.5 .times. 16 .mu. and the 2 openings exposing the base region are 3 .times. 20 .mu.. A 0.5 .mu. layer of Al is deposited over the whole surface. The Al layer is then selectively removed to leave an emitter contact layer in the form of a finger, 3 .mu. wide, which further extends over the Si **oxide layer** portions and terminates in a large area **bonding pad** on a Si **oxide layer** portion above the collector region, and a base contact layer in the form of 2 fingers, each 3 .mu. wide, which further extend over the Si **oxide layer** portions and terminate in a large area **bonding pad** on the Si **oxide layer** above the collector region. The slice is then subdivided into a plurality of transistor units, 350 .times. 350 .mu., which are then individually **mounted** on a header, connections to the emitter and base **bonding pads** are made by wire bonding and encapsulation is effected in a manner as conventionally used in a planar transistor manuf.

L14 ANSWER 1 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:850053 HCAPLUS
DN 136:127018
TI Reliability of multi-layer aluminum capped copper interconnect structures
AU Mercado, Lei; Radke, Robert; Ruston, Matthew; Tran, Tu Anh; Williams, Bill; Yong, Lois; Chen, Audi; Chen, Scott
CS Motorola Semiconductor Products Sector, Tempe, AZ, 85284, USA
SO IEEE/CPMT International Electronics Manufacturing Technology Symposium, 26th, Santa Clara, CA, United States, Oct. 2-3, 2000 (2000), 84-93
Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
CODEN: 69CAPS
DT Conference; (microfiche)
LA English
AB Driven for further Si redn., wireless applications use Cu interconnection and increase **metal layer** count from three to five layers. More aggressive ESD structures placed under the **bond pads** offer a significant opportunity for addnl. die area and cost redn. Capping Cu **bond pads** with Al was selected as the primary approach for probing and wire bonding Cu devices. There exists an integral relation between probe damage on the **bond pads** and the subsequent wire-bondability. As the pad geometry gets smaller, the ratio of the area of probe damage to the **bond pad** size will get proportionally larger, thereby reducing the available Al necessary to form reliable Au-Al intermetallic coverage. This paper will describe probe and assembly processes developed for a fine pitch three-**metal layer** Cu interconnect device with ESD structures placed under **bond pads**. The relation between probe conditions and wire-bondability were examd. Ball shear, wire rip and corresponding failure modes were evaluated at various read points of thermal aging studies to evaluate the integrity of ball bonds onto the metal **stack**. Reliability assessment was also performed. Based on the studies studying the relation among the pad structures, probe and wire bond quality, recommendations were derived to ensure high quality, stable and reliable bonds for fine pitch wire bonding on multi-layer Cu interconnect devices.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 2 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:525824 HCAPLUS
DN 135:234472
TI ESD protection under grounded-up **bond pads** in 0.13 .mu.m eight-level copper metal, fluorinated silicate glass low-k intermetal dielectric CMOS process technology
AU Chou, Kuo-Yu; Chen, Ming-Jer
CS Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan
SO IEEE Electron Device Letters (2001), 22(7), 342-344
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Electrostatic discharge (ESD) protection device under the grounded-up **bond pad** is investigated in 0.13 .mu.m full eight-level copper metal CMOS process technol. with fluorinated silicate glass (FSG) low-k intermetal dielec. (IMD). The bonding force and power produces no cracking and no noticeable change in the second breakdown trigger point

(Vt2, It2). High current I-V measured from the different level **metal layers stack** structures shows that (1) It2 depends very weakly on **metal layers** used, as expected due to certain junction power dissipation criterion and (2) Vt2 increases with the no. of **metal layers**. The origin of the latter is increased dynamic impedance for increased **metal layer** no., as clarified by a simple RC model. The model also yields the intrinsic second breakdown trigger current and voltage for the underlying ESD protection device. Successfully configuring ESD protection circuits under the **bond pads**, therefore, not only is wholly free from the traditional area consumption, but also can substantially relax design constraints, enabling much more flexible and robust ESD schemes for various applications.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 3 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:195171 HCAPLUS
DN 134:216069
TI Fabrication of a semiconductor device with resin bumps that serve as external connection terminals
IN Yonemochi, Kazuto; Yonemochi, Masahiro
PA Shinko Electric Industries Co., Ltd., Japan
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6204162	B1	20010320	US 1999-427933	19991027
PRAI	JP 1998-314738	A	19981105		

AB A method for producing a semiconductor device includes the following steps: forming a recess on a 1st side of a metal substrate; forming a film, made of a metal that is not dissolved by an etchant soln. which dissolves the metal substrate, on an inner surface of the recess; punch-pressing a region of the metal substrate that corresponds to an area of the **metal film** from a 2nd side of the metal substrate so that the area of the **metal film** formed on the inner surface of the recess becomes substantially flush with the 1st side of the metal substrate, thereby forming a **bonding pad** from an extending portion of the **metal film** that extends from the inner surface of the recess over the 1st side of the metal substrate; **mounting** the semiconductor chip on the 1st side; wire-bonding electrodes of the semiconductor chip and the **bonding pads**; sealing the 1st side of the metal substrate that includes the semiconductor chip, the bonding wire and the **metal film** with resin; and dissolving and removing the metal substrate by etching, thereby exposing the **metal film** formed on the inner surface of the recess.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:877219 HCAPLUS
DN 134:50076
TI Semiconductor devices having semiconductor chips and fabrication thereof for decreasing ground inductance and thermal resistance
IN Sugiyama, Toru

PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000349088	A2	20001215	JP 1999-161987	19990609

AB The title fabrication involves forming a Au-plated ground **metal layer** on a wafer, etching the wafer surface for forming dicing lines to expose a **bonding pad** metal, adhering semiconductor chips on the wafer on the rear side or on the other side of the Au ground **metal layer**, and providing signal wirings from the rear side. The process provides easy **mounting** of low-ground inductance and low-thermal resistance MIC chips on the package substrates.

L14 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:784429 HCAPLUS
DN 133:328507
TI Forming semiconductor metalization barrier in semiconductor device fabrication
IN Lopatin, Sergey D.; Pramanick, Shekhar; Brown, Dirk
PA Advanced Micro Devices, Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6144099	A	20001107	US 1999-282079	19990330
US 6344410	B1	20020205	US 2000-634025	20000808
PRAI US 1999-282079	A3	19990330		

AB A method of forming semiconductor metalization barrier in semiconductor device fabrication is disclosed. A **stack** of cobalt layer and cobalt tungsten layer is deposited on a copper **bonding pad**.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:433303 HCAPLUS
DN 133:36710
TI Method for forming vertical interconnect process for silicon segments with dielectric isolation in electronic packaging
IN Vindasius, Alfons; Sautter, Kenneth M.
PA Cubic Memory Inc., USA
SO U.S., 24 pp., Cont.-in-part of U.S. 5,675,180.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6080596	A	20000627	US 1997-920273	19970822
EP 766909	A1	19970409	EP 1995-923676	19950608
PRAI US 1994-265081	A2	19940623		

US 1995-376149 A3 19950120

AB A method for vertically interconnecting **stacks** of Si segments. Each segment includes a plurality of adjacent die on a semiconductor wafer. The plurality of die on a segment are interconnected on the segment using one or more **layers** of **metal** interconnects which extend to all four sides of the segment to provide edge **bonding pads** for external elec. connection points. After the die are interconnected, each segment is cut from the backside of the wafer using a bevel cut to provide four inwardly sloping edge walls on each of the segments. After the segments are cut from the wafer, the segments are placed on top of one another to form a **stack**. Vertically adjacent segments in the **stack** are elec. interconnected by applying elec. conductive epoxy to one or more sides of the **stack**. The inwardly sloping edge walls of each of the segments in the **stack** provide a recess which allows the elec. conductive epoxy to access the edge **bonding pads** and lateral circuits on each of the segments once the segments are **stacked**. A dielec. coating is applied to the die to provide a conformal coating to protect and insulate the die and a laser was used to ablate the area over the **bond pads** to remove the dielec. coating to provide for elec. connections to the **bond pads**.

RE.CNT 100 THERE ARE 100 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:317277 HCAPLUS
DN 132:328679
TI Chip-type electronic parts for **mounting** on printed circuit boards
IN Iemura, Tsutomu; Sato, Hisashi
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2000138130	A2	20000516	JP 1998-311646	19981102

AB In the electronic parts, terminal electrodes coated with elec. conducting polymer **layers** contg. **metal** powders are formed on both end parts of ceramic substrates having active devices. The electrodes are **bonded** to electrode **pads** of printed circuit boards via elec. conducting polymer adhesives. The electronic parts show high heat and migration resistance.

L14 ANSWER 8 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:674828 HCAPLUS
DN 132:17531
TI Reliability of electroless processed thin layered solder joints
AU Wang, L. C.; Mei, Z.; Dauskardt, R. H.
CS Department of Materials Science and Engineering, Stanford University, Stanford, CA, USA
SO Materials Research Society Symposium Proceedings (1999), 563(Materials Reliability in Microelectronics IX), 3-8
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal

LA English
AB There has recently been an increasing interest in using electroless processes to produce the **metal** thin **film** **stacks** that make up the **bond pads** in solder ball grid array (BGA) packages. Electroless processes produce a more uniform and better controlled film thickness, but the resulting metal **stacks** have exhibited less mech. reliability than that of traditional electrolytic **stacks**. This paper addresses a layered system consisting of a eutectic Sn-Pb solder sandwiched between **stacks** of Cu, Ni, and Au thin films. The samples were tested to det. cyclic fatigue behavior and fracture toughness values using traditional linear elastic fracture mechanics techniques. Surprisingly, fatigue crack propagation occurred in the middle of the solder layer even though the electroless interface was expected to be very weak. In contrast, fracture tests did appear to cause failure near an interface, but not necessarily at the electroless interface. Fracture toughness values measured for these samples were much lower than those reported for bulk metals. These results are discussed in terms of the microstructures present to det. possible relations between the microstructure of the solder joint and its fracture behavior.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 9 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:166808 HCAPLUS
DN 130:190443
TI Vertical interconnect process for silicon segments with thermally conductive epoxy preform
IN Vindasius, Alfons; Sautter, Kenneth M.
PA Cubic Memory, Inc., USA
SO PCT Int. Appl., 59 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9910925	A1	19990304	WO 1998-US16901	19980814

W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE,

AB An app. for vertically interconnecting **stacks** of silicon segments is disclosed. Each segment includes a plurality of adjacent die on a semiconductor wafer. The plurality of dies on a segment are interconnected on the segment using one or more **layers** of **metal** interconnects which extend to all four sides of the segment to provide edge **bonding pads** for external elec. connection points. After the dies are interconnected, each segment is cut from the backside of the wafer using a bevel cut to provide four inwardly sloping edge walls on each of the segments. After the segments are cut from the wafer, the segments are placed on top of one another to form a **stack**. Vertically adjacent segments in the **stack** are elec. interconnected by applying an elec. conductive epoxy resin to one or more sides of the **stack**. The inwardly sloping edge walls of each of the segments in the **stack** provide a recess which allows the elec. conductive epoxy resin to access the edge **bonding pads** and lateral circuits on each of the segments once the segments are **stacked**. A thermally conductive epoxy preform is provided between the **stack** of segments so that the **stack** of segments are epoxied together. In one embodiment, the thermally conductive epoxy preform includes a plurality of glass spheres randomly

distributed within the preform to maintain a distance between the **stack** of segments.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:141307 HCAPLUS
DN 130:176180
TI Vertical interconnect process for silicon segments with dielectric isolation
IN Vindasius, Alfons; Sautter, Kenneth M.
PA Cubic Memory, Inc., USA
SO PCT Int. Appl., 57 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9909599	A2	19990225	WO 1998-US16900	19980814
	W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	US 6080596	A	20000627	US 1997-920273	19970822
	AU 9891976	A1	19990308	AU 1998-91976	19980814
	EP 1029360	A2	20000823	EP 1998-944438	19980814
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
	JP 2001516148	T2	20010925	JP 2000-510170	19980814
PRAI	US 1997-915620	A	19970821		
	US 1997-920273	A	19970822		
	US 1994-265081	A2	19940623		
	WO 1998-US16900	W	19980814		

AB In vertically interconnecting **stacks** of Si segments, each of which includes a plurality of adjacent dice on a semiconductor wafer, the plurality of dice on a segment are interconnected on the segment using .gtoreq.1 **layers** of **metal** interconnects which extend to all 4 sides of the segment to provide edge **bonding pads** for external elec. connection points. After the dice are interconnected, each segment is cut from the backside of the wafer using a bevel cut to provide 4 inwardly sloping walls on each of the segments. After the segments are cut from the wafer, the segments are placed on top of each other to form a **stack**. Vertically adjacent segments in the **stack** are elec. interconnected by applying elec. conductive epoxy to .gtoreq.1 sides of the **stack**. The inwardly sloping walls of each of the segments in the **stack** provide a recess which allows the elec. conductive epoxy to access the edge **bonding pads** and lateral circuits on each of the segments once the segments are **stacked**. A dielec. coating is applied to the dice to provide a conformal coating to protect and insulate the dice and a laser is used to ablate the area over the **bond pads** to remove the dielec. coating to provide for elec. connections to **bond pads**.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:487899 HCAPLUS
DN 122:228668
TI **Mounting** semiconductor devices
IN Mori, Miki; Saito, Masayuki; Iwase, Nobuo
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06252148	A2	19940909	JP 1993-35695	19930224

AB **Bonding pads** of semiconductor devices and circuits (e.g., Al) are connected across In/Pb bumps, and nickel-coated resin balls.

L14 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:100556 HCAPLUS
DN 104:100556
TI Anisotropically conductive adhesive composition
IN Dery, Ronald Allen; Jones, Warren Charlie; Lynn, William Joseph; Rowlette, John Robert
PA AMP Inc., USA
SO PCT Int. Appl., 31 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 8504980	A1	19851107	WO 1985-US477	19850416
W: JP, KR				
RW: AT, BE, CH, DE, FR, GB, IT, LU, NL, SE				
EP 179805	A1	19860507	EP 1985-901804	19850416
R: CH, DE, FR, GB, IT, LI, NL, SE				
JP 61501924	T2	19860904	JP 1985-501698	19850416
PRAI US 1984-601836		19840419		
US 1985-710361		19850314		
WO 1985-US477		19850416		

AB An anisotropic conductive adhesive compn., consisting of conductive particles and a nonconductive adhesive binder, is prepd. to adhere a conductive area on a substrate to a conductive area on another substrate for elec. connection. The conductive particles are **metallic**, **metal-coated** nonconductive base, or conductive nonmetal particles coated with Au, Ag, Pd, Pt, or Rh and have particle sizes neither fine nor large. The nonconductive adhesive is a pressure-sensitive, hot melt, or polymerizable adhesive. The particles are randomly dispersed in the adhesive and form clusters so as to form noncontiguous conductive units sufficiently spaced apart to preclude elec. conduction between adjacent conductive areas on the substrate when applied for adhesion. Insulation resistance measurements showed that particle contents of 3-15% by vol. are acceptable. Any suitable method is adopted in application of the compn. Thus, 2.59 g Pd-coated Ni flakes of 16.4 .times. 11.7 .times. 6 .mu. av. size were mixed with 25 g Adcote 72A106 rubber-base pressure-sensitive adhesive and 0.5 wt.% Inmont RW 0158 flow

modifier. A 0.02-mm-thick 2.54-cm square adhesive film pad sandwiched by 2 silicone-coated release papers and 2 polyester film strips having 5 screen-printed Ag ink traces were prepd. Lap joints were made by **bonding** the adhesive **pad** on a polyester film and then another polyester film on another side of the adhesive pad on a designated area. Lap shear tests and 180.degree. peel tests were made at -40.degree., 20.degree. and 80.degree., e.g., 7.38 kg/cm2 for the lap shear and 339 g/cm for a force to initiate peeling in the 180.degree. peel test at 20.degree.. Joint efficiency (joint conductance/theor. joint conductance) was 66% with a joint resistance of 0.79 .+-. 0.11 .OMEGA.. The compn. is applied to interconnection of conductive areas, e.g., silk-screened inks and electrodeposited inks, on flexible substrates or circuit boards, or to **mounting** of component parts on circuit traces.

L14 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1983:431816 HCAPLUS
DN 99:31816
TI Multicomponent-semiconductor device
PA Fujitsu Ltd., Japan
SO Jpn. Tokkyo Koho, 4 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 58007074	B4	19830208	JP 1975-129690	19751028

AB The fabrication of a multicomponent semiconductor device (e.g., a HgCdTe photoconductive device) involves the following steps: (1) forming a groove in an insulator substrate; (2) **mounting** a multicomponent-semiconductor element in the groove; (3) polishing the surfaces of the substrate and element to form planar surfaces; and (4) depositing a **metal film** over the element excluding the photoreceiving surfaces and the protruding regions at both sides of the groove to form **bonding pads**. Alternatively, the element may be **mounted** on an insulator substrate and a support substrate may be provided on both sides of the element.

L14 ANSWER 14 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1982:44799 HCAPLUS
DN 96:44799
TI Hermetic chip carrier process and materials development
AU Caswell, Greg; Isaacson, Dale
CS Tracor, Inc., Austin, TX, USA
SO Proc. Tech. Program - Int. Microelectron. Conf. (1981) 237-47
CODEN: PPICDF; ISSN: 0163-917X
DT Journal
LA English
AB The suitability of different materials for forming large-scale integrated circuits on the basis of hermetic-chip carrier (HCC) packaging was studied with mech. and environmental testing. The sides of the HCC have vertical castellations and metalized grooves to connect the **bonding pads** on their bottoms to corresponding substrate pads. These devices are **mounted** in interconnect structures to form the microcircuit module. Al2O3 and porcelain steel substrates were tested along with different solder pastes for assembling the circuit. The strongest pastes contained Ag. Pretinning of HCC's with Sn-37% Pb solder was required for max. strength. Bonding to substrate metalizations of

Pt-Au and Pd-Ag was essentially identical for different mech. and environmental stresses. Porcelain steel appears to be as good as Al2O3 as a substrate.

L16 ANSWER 1 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:363860 HCAPLUS
DN 135:100794
TI A correlation between highly accelerated wafer level and standard package level electromigration tests on deep sub-micron via-line structures
AU Lepper, M.; Bauer, R.; Zitzelsberger, A. E.
CS Reliability Methodology, Infineon Technologies AG, Munich, D-81739, Germany
SO IEEE International Integrated Reliability Workshop Final Report, 19th, Lake Tahoe, CA, United States, Oct. 23-26, 2000 (2000), 70-73 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y. CODEN: 69BICY
DT Conference
LA English
AB So far little trust was put in lifetime projections from highly accelerated Wafer Level electromigration tests on deep sub-micron via-line structures. This was mainly due to a missing correlation between the highly accelerated Wafer Level tests and the conventional Package Level stress technique. The authors used a const. current stress mode for both, Package Level and Wafer Level, and compared the electromigration test results. The lifetime projection to operating conditions revealed a good correlation between them. Hence the authors' procedure is to be regarded as a promising tool to ensure rapid and cost-effective reliability feedback during technol. development.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L16 ANSWER 2 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:736238 HCAPLUS
DN 133:289968
TI Self aligned dual damascene fabrication process for interconnect conducting lines and via contacts with low parasitic capacitance
IN Tsai, Ming-Hsing; Shue, Shau-Lin
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6133144	A	20001017	US 1999-368864	19990806

AB An improved and novel process for fabricating unique interconnect conducting lines and via contact structures was developed. Using this special self aligned dual damascene process, special interconnect conducting lines and via contacts are formed which have low parasitic capacitance (low RC time consts.). The invention incorporates the use of double etch stop or etch barrier layers. The key process step of this invention is special patterning of the etch stop or etch barrier layer. This is the advantage of this invention over Prior Art processes that need a continuous, thick stop layer that has a etching selectivity to SiO2, SiO2 (increasing parasitic capacitance). However, in this invention a self aligned dual damascene process and structure is presented that is easier to process and has low parasitic capacitance. Repeating the self aligned dual damascene processing steps, constructs multilevel conducting structures. This process reduces processing time, reduces the cost of ownership, (compatible with low dielec. const. materials) and at the same time produces a product with superior lines and via contact structures

(using special etch stop or etch barrier layer patterning), hence improving reliability.

L16 ANSWER 3 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:482103 HCAPLUS
DN 133:201351
TI An in-line contact and via hole inspection method using electron beam compensation current
AU Yamada, Keizo; Nakamura, Toyokazu; Tsujide, Tohru
CS Device Analysis Technology Labs, NEC Corporation, Kanagawa, Japan
SO Technical Digest - International Electron Devices Meeting (1999) 483-486
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB In-line contact and via hole inspection technol. will play a vital role in ensuring accelerated yield ramps and quickly identifying and resolving yield excursions in the SOC era. The authors have developed an in-line contact and via hole inspection method using electron beam compensation current. This method will provide a nondestructive contact and via hole inspection tool with a thickness measurement capability for the hole bottom nm order SiO2 film and the hole diam. measurement capability as well as performing a superhigh inspection speed at over 1000 times faster than a SEM-based method.

L16 ANSWER 5 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:282381 HCAPLUS
DN 128:329736
TI Method for forming conductive lines and stacked vias for integrated circuit
IN Chen, Li-chun; Shen, Chih-heng
PA Taiwan Semiconductor Manufacturing Company Ltd, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5747383	A	19980505	US 1995-523329	19950905

AB A method for fabricating an improved connection between active device regions in silicon, to overlying metalization levels, has been developed. A LPCVD tungsten contact plug process, which results in optimum coplanarity between the top surface of the tungsten plug and the surrounding insulator surface, has been created.

L16 ANSWER 6 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:298197 HCAPLUS
DN 124:329972
TI Surface-diffused high-aspect-ratio/low-resistance electric wires and via-connectors and manufacture of transistor circuits using thereof
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 08064599	A2	19960308	JP 1995-196745	19950801
	JP 3083735	B2	20000904		
	EP 915501	A1	19990512	EP 1999-101825	19950705
	R: DE, FR, GB				
	US 5856026	A	19990105	US 1996-603092	19960220
	US 5731245	A	19980324	US 1996-738901	19961028
	US 5897370	A	19990427	US 1996-738883	19961028
	US 5877084	A	19990302	US 1997-941062	19970930
PRAI	US 1994-286605	A	19940805		
	US 1995-479406	A3	19950607		
	EP 1995-110478	A3	19950705		

AB The metalization process in the title manufg. employs vapor deposition with Ge hydrides to give Ge alloys contg. Al, Au, or Ag. The Ge alloys provide a passivation layer in prevention of voids and side-seams for via hole deposition and high-aspect-ratio circuit wiring in FETs and BiCMOS transistors.

L16 ANSWER 8 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:43735 HCAPLUS
DN 120:43735
TI Refractory metal-capped low-resistivity metal conductor lines and vias
IN Cote, William J.; Lee, Pei Ing P.; Sandwick, Thomas E.; Vollmer, Bernd M.; Vynorius, Victor; Wolff, Stuart H.
PA International Business Machines Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5262354	A	19931116	US 1992-841693	19920226
	KR 9706973	B1	19970501	KR 1993-763	19930121
	JP 06084826	A2	19940325	JP 1993-16123	19930203
	JP 2989408	B2	19991213		
	CN 1076547	A	19930922	CN 1993-101334	19930224
	EP 558004	A2	19930901	EP 1993-102979	19930225
	EP 558004	A3	19940112		
	EP 558004	B1	19971022		
	R: AT, DE, FR, GB, IE, IT, NL				
	AT 159615	E	19971115	AT 1993-102979	19930225
PRAI	US 1992-841693	A	19920226		

AB Elec. conducting vias and lines are created by a three step process. First, a controlled amt. of a soft, low-resistivity metal is deposited in a trench or hole to a point below the top surface of the dielec. in which the trench or hole is formed. Subsequently, the low-resistivity metal is overcoated with a hard metal such as CVD W. Finally, chem.-mech. polishing is used to planarize the structure. The hard metal protects the low-resistivity metal from scratches and corrosion which would ordinarily occur if the low-resistivity metal were subjected to the harsh chem.-mech. polishing slurries.

L16 ANSWER 14 OF 15 HCAPLUS COPYRIGHT 2002 ACS
AN 1976:93757 HCAPLUS
DN 84:93757
TI Fabrication techniques for tungsten cat whisker infrared antennas
AU Twu, Bor-Long
CS Dep. Electr. Eng. Comput. Sci., Univ. California, Berkeley, Calif., USA

SO J. Electrochem. Soc. (1975), 122(11), 1560-1
CODEN: JESOAN
DT Journal
LA English
AB Conical W [**7440-33-7**] wires 40-170.mu. long were prepd. by electrochem. etching for W point contact diodes of ir antennas. The conical shapes were obtained by etching near the electrolyte surface and by passing d.c. from a 25.mu. diam. W **wire through** 0.18-0.75N NaOH soln. to a Pt cathode. The longest cones were obtained in the most dil. solns.

L18 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:744667 HCAPLUS
DN 135:265778
TI **Bond pad** having vias usable with antifuse process technology
IN Wong, Richard J.
PA Quicklogic Corp., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6300688	B1	20011009	US 1994-350865	19941207

AB A lower **metal plate** having a strip-like opening was used in a **bond pad** structure having metal plugs coupling the lower **metal plate** to an upper **metal plate**. A vol. of relatively rigid material filling a vol. above the strip-like opening transfers stress from the upper **metal plate**, through the strip-like opening, and to a foundation layer upon which the lower **metal plate** is disposed. The **bond pad** structure can be fabricated using the same semiconductor processing steps used to fabricate amorphous silicon antifuse structures having metal plugs.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L18 ANSWER 2 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:241819 HCAPLUS
DN 134:260183
TI Micromachined variable capacitor
IN Gammel, Peter Ledel; Walker, James Albert
PA Lucent Technologies Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6212056	B1	20010403	US 1999-280804	19990326

AB First and 2nd wafers are micromachined by std. integrated-circuit fabrication techniques to resp. make 1st and 2nd component parts of a variable capacitor. A thin flexible membrane in the 1st wafer is integral with and mech. supported by the 1st wafer. A metal pattern on the 1st wafer includes a 1st capacitor plate on the membrane. In the 2nd wafer, a well is formed. A metal pattern on the 2nd wafer includes a 2nd capacitor plate in the well. By bonding the 2 parts together face-to-face, the capacitor plates are positioned in spaced-apart alignment with each other. External elec. connections to the plates are made via **bonding-pad** portions of the metal patterns on the wafers. In response to elec. control signals, the **metal plate** on the membrane can be moved toward the other plate, thereby selectively changing the capacitance of the assembly.

L18 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:539770 HCAPLUS
DN 133:128685
TI Leadframes and fabrication of polymer-sealed semiconductor devices using thereof
IN Minamio, Masaki; Araki, Masanao; Takazaki, Shuji; Nakazawa, Eiichi; Ono, Takashi
PA Matsushita Electronics Corp., Japan
SO Jpn. Tokkyo Koho, 21 pp.
CODEN: JTXXFF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 3046024	B1	20000529	JP 1999-115899	19990423
JP 2000307045	A2	20001102		

AB The title leadframes comprise (1) a **metal plate** frame body, (2) a semiconductor component-mounting die pad attached with projections on the surface and provided in the frame body, (3) a suspending lead supporting a die pad on its one end and connecting to the frame at its the other end, (4) a lead having a **bonding pad** connected to a metal filament on its one end and to a frame at its the other to provide a land electrode on its bottom surface, and (5) land lead provided with an extended end toward the die pad side on one side of the edge of the lead and connected to the frame on the other side with its bottom to become a land electrode. The arrangement prevents formation of plastic burr on the land electrode.

L18 ANSWER 6 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:362983 HCAPLUS
DN 133:11859
TI Printed circuit board for plastic-packaged semiconductor device
IN Oka, Morio; Ikeguchi, Nobuyuki; Kobayashi, Toshihiko
PA Mitsubishi Gas Chemical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000150714	A2	20000530	JP 1998-333452	19981109

AB The circuit board involves an inserted **metal plate**, with the similar size as the board, placed at the middle of the thickness and the **metal plate** has bumps, which are elec. connected to a Cu layer formed on the surface of semiconductor chips on the board and another Cu layer on the opposite side of the board having heat-releasing solder ball pads. The semiconductor chips are bonded on the board by a heat-conductive adhesive, the inserted **metal plate** is elec. insulated with elec. circuits on the surface of the board by intermediate thermosetting resin layers, the semiconductor chips and the circuits are connected by wire bonding, elec. conductors involved in the boards are connected by through holes, and the semiconductor chips, wires, and **bonding pads** are packaged with a plastic. So-called popcorn phenomena, i.e., blister under heat in mounting the board on mother board, etc., is prevented.

L18 ANSWER 7 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:818233 HCAPLUS

DN 132:57959
TI Wafer level fabrication and assembly of chip scale packages
IN Farnworth, Warren M.
PA Micron Technology, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6008070	A	19991228	US 1998-82745	19980521
	US 6326697	B1	20011204	US 1998-208906	19981210
	US 6284573	B1	20010904	US 1999-388033	19990901
	US 2002001922	A1	20020103	US 2001-920970	20010802
PRAI	US 1998-82745	A3	19980521		
	US 1999-388033	A1	19990901		

AB The invention relates to a process for making integrated circuit devices, comprising the steps of forming and packaging such devices at the wafer scale, including forming a plurality of chip circuits with **bond pads**, adhesively fixing a plate of glass to the active surface of the wafer, slicing the wafer, applying a sealant layer to the backside of the wafer, forming contact holes through the upper glass **plate**, **metalizing** the glass **plate** and isolating the individual chips. Use of etchable glass for the package and palladium for metalization provides an advantageous construction method.

L18 ANSWER 9 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:93048 HCAPLUS
DN 120:93048
TI Metalized paths on diamond surfaces
IN Dautremont-Smith, William C.; Feldman, Leonard C.; Kalish, Rafael; Katz, Avishay; Miller, Barry; Moriya, Netzer
PA American Telephone and Telegraph Co., USA
SO Can. Pat. Appl., 17 pp.
CODEN: CPXXEB
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	CA 2084147	AA	19930612	CA 1992-2084147	19921130
	US 5334306	A	19940802	US 1992-973611	19921119
PRAI	US 1991-806934		19911211		
	US 1992-870741		19920417		
	US 1992-927772		19920810		
	US 1992-973611		19921119		

AB A graphite path is formed along the surface of a diamond plate, preferably a CVD diamond plate, by means of a laser. The path advantageously can be the surface of a sidewall of a via hole drilled by the laser through the plate or a path running along a side surface of the **plate** is **metalized**, as by electroplating. In this way, e.g., an elec. conducting connection can be made between a metalized backplane located on the bottom surface of the plate and a wire-**bonding pad** located on the top surface of the plate.

L22 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:10848 HCAPLUS
DN 136:94468
TI Process for making miniature micro-device package
IN Jerominek, Hubert; Alain, Christine
PA Institut National D'Optique, Can.
SO PCT Int. Appl., 49 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2002001633	A1	20020103	WO 2001-CA939	20010627

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI CA 2000-2312646 A 20000628
AB The present invention is concerned with a miniature micro-device package and a process of making thereof. The package has a miniature frame substrate made of a material selected form the group including: ceramic, metal and a combination of ceramic and metal. The miniature frame substrate has a spacer delimiting a hollow. The package also includes a micro-device die having a micro-device substrate , a micro-device integrated on the micro-device substrate, **bonding pads** integrated on the micro-device substrate, and elec. conductors integrated in the micro-device substrate for elec. connecting the **bonding pads** with the micro-device. The micro-device die is **mounted** on the spacer to form a chamber. The micro-device is located within the chamber. The **bonding pads** are located outside of the chamber.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:437334 HCAPLUS
DN 129:196254
TI Effect of Al3Ti intermetallic compound on electromigration lifetime of Al alloy interconnections
AU Kouno, T.; Hosaka, M.; Niwa, H.; Yamada, M.
CS ULSI Development Division, Fujitsu Limited, 4-1-1 Kami-kodanaka, Nakahara-ku, Kawasaki, 211-8588, Japan
SO J. Appl. Phys. (1998), 84(2), 742-750
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB The dependence of the electromigration (EM) lifetime and the cross-sectional structure of interconnections after EM tests on linewidths was studied in multi-level and single-level Al alloy interconnections consisting of a top-TiN/Ti/Al-0.5%Cu/TiN/Ti-bottom **stack**. An almost uniform Al3Ti intermetallic compd. layer was formed by a known

reaction between the Ti and Al. The authors found the following anomalous behavior: the mean time to failure (MTF) of EM in the multi-level interconnections with **tungsten** diffusion barriers decreased by increasing the linewidth. Also in the multi-level interconnections after EM tests, independent of linewidths, a local Al thickening formed near the anode end of the line and voids formed near the cathode end. However, in the single-level interconnections with **bonding pads**, the MTF of EM increased by increasing the linewidth and, after EM tests, a local Al thickening formed near the anode end even though no voids were obsd. near the cathode end. This directly opposed EM lifetime dependency on linewidth found in the multi-level and single-level interconnections and the obsd. Al thickening correlate closely with the fast diffusivity of Al atoms at the interface between the Al3Ti and Al and/or between the Al3Ti and TiN.

L22 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:128010 HCAPLUS
DN 126:219674
TI Fabricating field-emission device metalization
IN Shen, Chi-cheong; Hodson, Lester L.
PA Texas Instruments Incorporated, USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5601466	A	19970211	US 1995-424833	19950419
	JP 09097559	A2	19970408	JP 1996-98780	19960419
PRAI	US 1995-424833		19950419		

AB The fabrication of an emitter plate having Ti-W and Al used in a sublayering arrangement as the metalization material for the gate electrodes, cathodes, **bond pads**, interconnects, and integrated circuit **mounting** pads is described. In 1 embodiment, Ti-W and Al sublayers are combined with Nb to provide the metalization material.

L22 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:634932 HCAPLUS
DN 123:90164
TI Reliable Au-Sn flip chip bonding on flexible prints
AU Baggerman, A. F. J.; Batenburg, M. J.
CS Philips' Centre Manufacturing Technology, Eindhoven, 5600 MD, Neth.
SO Proc. - Electron. Compon. Technol. Conf. (1994), 44th, 900-5
CODEN: PETCES
DT Journal
LA English
AB Au-Sn flip chip bonding is successfully introduced for the **mounting** of integrated circuits on flexible polyimide prints. Flip chip was used, since in most consumer electronics, and, more specific for hearing instruments, the useable vol. is decreasing very rapidly. Since on the same flex print reflow soldering of other components is required, a high melting soldering process is preferred. An addnl. advantage of the Au-Sn process is that the bumps do not completely melt, and a certain stand off height is guaranteed. The bumps are deposited on top of the **bond pads** and are **bonded** to Cu tracks on a polyimide foil. The required Sn is either deposited on the bump or on the Cu tracks. Both Au-Sn soldering processes are performed by

using pulsed heat thermode (gang) bonding. It is found that the quality of the bonds depends on the microstructure formed in the bonding region. EDX measurements indicate that for good quality bonds eutectic (80/20) Au-Sn or .zeta.' phases are required. To obtain these phases the temp. at the interface and the initial amt. of Sn are optimized.

L22 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:626912 HCAPLUS
DN 123:242984
TI Inner lead gang-bonded devices with **stacked** Ni-Au bumps
AU Baggerman, Antal F. J.; van Gerven, Jo A. H.
CS Philips Centre for Manufacturing Technology, Eindhoven, Neth.
SO IEEE Trans. Compon., Packag., Manuf. Technol., Part B (1995), 18(2), 366-74
CODEN: IMTBE4; ISSN: 1070-9894
DT Journal
LA English
AB Tape automated bonding (TAB) is a technique which was characterized by a small lead pitch, a small size, and a good high frequency behavior. To bond the inner leads of the TAB foil on the straight wall bumps on the integrated circuit (IC), thermocompression gang bonding is usually applied. If simple thin Si nitride passivation layers were used, cracks are often obsd. in the sputtered TiW barrier layer (beneath the bump) and in the passivation layer of the IC. A theor. model was used to describe the deformation of the bump-lead structure. Comparison of this model with exptl. results of the cracking behavior shows that both stress and strain at the **bond pad**-bump interface exceed the crit. values for cracking. Plastic deformation at the bondpad is avoided if a two layer Ni-Au bump structure was used. While the plastic deformation required at the bond interface is kept const., Ni layers with a thickness of at least 10 .mu.m are required to avoid even the smallest cracks. If the Au layer thickness is at least 15 .mu.m, the resulting bond strength is comparable with that of std. Au bumps. Deformation of the leads is restricted within acceptable limits, and the long-term reliability is not affected. Accelerated testing was performed by high temp. storage, pressure cooker and air-to-air temp. shock testing.

L25 ANSWER 1 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:163835 HCAPLUS
DN 136:209185
TI Method of fabricating direct contact through hole type wafer on both sides of the chip in semiconductor package
IN Hsuan, Min-chih; Han, Charlie
PA United Microelectronics Corp., Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6352923	B1	20020305	US 1999-260219	19990301

AB A method of fabricating a direct contact through hole type wafer and fabricating a wafer-level package with reduced vol. and height. Devices and contact plugs are formed in one side of a Si-on-insulator substrate, and multilevel interconnects are formed over the side of the Si-on-insulator substrate. The multilevel interconnects are coupled with the devices and the contact plugs. **Bonding pads**, which couple with the multilevel interconnects, are formed over the multilevel interconnects. An opening is formed on the other side of the Si-on-insulator substrate to expose the contact plugs. An **insulation layer**, a barrier **layer** and a **metal layer** are formed in sequence in the opening. Bumps are formed on the **bonding pads** and the **metal layer**, resp.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 2 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:868983 HCAPLUS
DN 135:379571
TI Method for reworking **metal layers** on integrated circuit **bond pads** without damaging the **metals** or dielectric **layers**
IN Stierman, Roger J.; Moore, Thomas M.; Shinn, Gregory B.
PA USA
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001046721	A1	20011129	US 2001-832968	20010411
PRAI US 2000-196705P	P	20000413		

AB A method for reworking integrated circuit (IC) wafers having Cu-metalized **bond pads** exposed in protective overcoat openings and one or more bondable **metal layers** deposited onto the **bond pads** by a technol. which may produce some parts with off-spec or missing depositions. After identifying the wafer with off-spec **metal layers**, a **layer** of glass buffer is deposited over those wafers, which also fill any missing depositions at least partially. The glass-covered surface is then chem.-mech. polished until the off-spec **metal layers** and at least portion of the protective overcoat are removed, without

damaging the Cu metalization. Finally, a fresh layer of protective overcoat is deposited, selectively opened to expose the **bond pads**, and provided anew with one or more bondable **metal layers**. The slurry for the chem.-mech. polishing contains oxidizing or hydroxylating agents as well as mech. polishing components for metals which are not readily oxidized. In order to minimize undesired scratches of the underlying Cu or dielec. layers, a combination of buffers and soft poromeric pads was used. Alternatively, org. buffer layers can be used instead of the glass buffer.

L25 ANSWER 3 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:703763 HCAPLUS
DN 135:235008
TI Process for controlling oxide thickness over a fusible link using transient etch stops
IN Tzeng, Wen-Tsing; Chen, Yue-Feng; Wang, Kau-Jan
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6294474	B1	20010925	US 1999-425906	19991025

AB A method is described for progressively forming a fuse access opening for laser trimming in an integrated circuit with improved control of dielec. thickness over the fuse. A dielec. layer is formed over the fuse and a polysilicon layer is then patterned over the fuse to form a 1st etch stop. An inter-level dielec. (ILD) layer is added and a 2nd etch stop is formed in a 1st **metal layer** on the ILD layer over the 1st etch stop. The 2nd etch stop serves to protect the ILD layer over the fuse from being etched by an ARC over etch during the via etching in a 1st inter-**metal** dielec. (IMD) **layer**. A 1st portion of the laser access window is formed during the via etching of the 1st IMD layer. The 2nd etch stop is then removed by the 2nd metal patterning etch, exposing the ILD layer over the 1st etch stop at it's original thickness. A passivation layer is deposited and patterned to form access openings to **bonding pads** as well as to further open the laser access window to the 1st etch stop. The 1st etch stop prevents penetration of the subjacent **insulative layer** over the fuse, thereby maintaining a controlled uniform thickness of that layer. When the **bonding pads** are opened, including the removal of an ARC on their surface, the etchant conditions are changed to remove the etch stop and subsequently a portion of the subjacent **insulative layer** over the fuse leaving a precise and uniform thickness of dielec. material over the fuse. The process fits conveniently within the framework of an existing process and does not introduce any addnl. steps.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 4 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:499837 HCAPLUS
DN 135:85582
TI Process for low-constant dielectric with metal dummy plugs for stress relief by providing thermal conductivity
IN Yu, Chen-hua; Jeng, Shwangming
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 9 pp.

CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6258715	B1	20010710	US 1999-228125	19990111

AB Low dielec. inter-**metal** dielec. (IMD) **layers** made of H silsesquioxane (HSQ) or Me silsesquioxane (MSQ) spin-on-glass do not have good thermal cond. as compared to regular oxides and the adhesion of HSQ or MSQ is worse than that of **oxide** to **oxide layers**. Methods are disclosed and illustrated to improve the heat transfer by providing metal dummy plugs under and/or around **bonding pads** or between **metalization layers**. The arrangement and nos. of dummy plugs depends on the heat to be transferred and varies with the application. Good thermal cond. is of particular importance because the effects of high local temp. around **bonding pads** during chip **bonding** results in thermal stress and delamination of the IMD layers. The use of **bonding pads** provides other benefits as well.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 5 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:469579 HCAPLUS
DN 135:69548
TI Semiconductor devices having stable component isolation
IN Naruke, Kiyomi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001176874	A2	20010629	JP 1999-356079	19991215

AB The title devices comprise a Si substrate, a MOS transistor formed on component regions, a shallow trench isolation (STI) region in isolating between the component regions, an interlayer **insulator film** over the entire surface, and a **metal** circuit **layer** and **metal bonding pad** formed on the **insulator film** and connected to the MOS transistors through contact holes to the **insulator film**. A bonding region is provided below the **bonding pad** on the substrate for not providing STI regions nor semiconductor components. The device structure gives the multilayer circuit-semiconductor devices stable component isolation for fine integration and circuit reliability.

L25 ANSWER 6 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:356758 HCAPLUS
DN 134:374841
TI Semiconductor devices and their production method for preventing a **bonding pad** from peeling off from a first conducting **layer** and an **insulator layer**
IN Maema, Tetsuya; Komuro, Masamichi
PA Hitachi Ltd., Japan; Hitachi Super LSI System Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 7 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001135639	A2	20010518	JP 1999-314707	19991105

AB The title method includes forming a first conducting layer which is composed of plural polycryst. Si pieces arranged in the lattice shape and forming a barrier **metal layer** made of high melting-point metals, metal silicides, or metal nitrides, between the first conducting layer and a **bonding pad** (a second conducting layer) made of aluminum alloy and between the **bonding pad** and a first **insulator layer**. Alternatively, the polycryst. Si pieces can have an uneven surface.

L25 ANSWER 7 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73502 HCAPLUS
DN 134:124771
TI Passivation layer etching process for memory arrays with fusible links
IN Tzeng, Wen-Tsing; Yang, Chun-Pin; Lin, Hsing-Lien
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6180503	B1	20010130	US 1999-354852	19990729

AB A method is described for progressively forming a fuse access openings in integrated circuits which are built with redundancy and use laser trimming to remove and insert circuit sections. The fuses are formed in a polysilicon layer and covered by .gtoreq.1 relatively thin **insulative layers**. An etch stop is patterned over the fuse in a higher level polysilicon layer or a 1st **metalization layer**. Addnl. **insulative layers** such as inter-**metal** dielec. **layers** are then formed over the etch stop. A 1st portion of the laser access window is then etched during the via etch for the top metalization level. The etch stop prevents removal of the insulation subjacent to it. Cumulative thickness non-uniformities in the relatively thick upper **insulative layers** are thus removed from the fuse window. The etch stop is removed during patterning of the top level metalization. A passivation layer is applied and patterned to exposed **bonding pads** and, at the same time complete the etching of the laser access window to a desired thickness over the fuses. The passivation layer over etch required to penetrate the **insulation layer** over the fuses also removes an antireflective coating over the **bonding pads**. The process fit conveniently within the framework of an existing process and does not introduce any addnl. steps. In addn., the passivation layer can be patterned to form final access to both **bonding pads** and laser access openings with a single photolithog. mask.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 8 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:29151 HCAPLUS

DN 134:94309
TI Semiconductor devices having multilayer circuits in prevention of cracks in **bonding pads**
IN Idemitsu, Hajime
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001007113	A2	20010112	JP 1999-178454	19990624

AB The title devices comprise a 1st metal circuit and a metal pattern both buried deep in floating in a thick **insulator film** provided on a semiconductor substrate, a **bonding pad** formed on the **insulator film** in a position in opposed to the metal pattern, a 2nd metal circuit formed in the insulator in a depth between the 1st metal circuit and the metal pattern, and a via hole interconnect connecting the 1st and 2nd metal circuits and the metal pattern. The circuit arrangement prevents development of cracks other wise stretched up to the **bonding pad**.

L25 ANSWER 9 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:622448 HCAPLUS
DN 133:186700
TI Wafer structure for securing **bonding pads** on integrated circuit chips and a method for fabricating the wafer structure
IN Chen, Kun-Cho; Jenq, Jason
PA United Microelectronics Corp., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6114231	A	20000905	US 1996-691522	19960802
PRAI TW 1996-85105359	A	19960506		

AB A wafer structure on an IC chip allows the **bonding pads** on the IC chip to be firmly secured to the IC chip, thereby preventing detachment of the **bonding pads** during assembly of the IC package. The wafer structure comprises a substrate on which at least a pad area is defined. The pad area is formed with a 1st **insulating layer**, a gate on the 1st **insulating layer**, a 2nd **insulating layer** on the gate, and a 3rd **insulating layer** on the 2nd **insulating layer**. The 2nd **insulating layer** has a plurality of lower openings formed there through and the 3rd **insulating layer** has a plurality of upper openings formed there through, each upper opening corresponding to one of the lower openings. The lower openings are wider than the upper openings. Plugs are formed in the lower and upper openings and are bonded to a **metalization layer** which serves as a **bonding pad** for the IC chip. The wider lower part of the plugs allows them to be rigidly affixed within the openings, thus allowing the overlaying **bonding pad** to be firmly secured to the IC chip. Therefore, during assembly of the IC chip, the **bonding pad** is not readily detached from the IC chip, thus increasing the

assembly yield of good IC packages.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 10 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:121625 HCAPLUS
DN 132:159038
TI Pad definition to achieve highly reflective plate without affecting bondability
IN Wong, George
PA Chartered Semiconductor Manufacturing, Ltd., Singapore
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6027999	A	20000222	US 1998-151159	19980910
	JP 2000174058	A2	20000623	JP 1999-257382	19990910
PRAI	US 1998-151159	A	19980910		

AB Fabrication is described of pixels and **bonding pads** (at the metal level below the reflective layer) in prodn. of liq. crystal display (LCD) integrated circuit device. In this process semiconductor device structures are formed in and on a semiconductor substrate and covered by an **insulating layer**. A first **metal layer** is deposited overlying the **insulating layer** and patterned to form a metal line and a **bonding pad**. A dielec. layer is deposited overlying the metal line and the **bonding pad**. Vias are opened through the dielec. **layer** to the **metal** line but not to the **bonding pad**. A second **metal layer** is deposited overlying the dielec. layer and filling the via openings and etched back to form metal plugs. A third **metal layer** is deposited overlying the dielec. **layer** and **metal** plugs and patterned to form pixels contacting metal plugs. A passivation layer is deposited overlying the pixels. A via opening is etched through the passivation layer and the dielec. layer to the **bonding pad**. A wire bond is formed within the via opening to contact the **bonding pad** to complete the fabrication of the integrated circuit device.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 11-20

L25 ANSWER 11 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:430683 HCAPLUS
DN 131:81535
TI Fabrication of a semiconductor integrated circuit device
IN Ohnuma, Manabu
PA NEC Yamagata, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 11186269	A2	19990709	JP 1997-355069	19971224

AB The invention relates to a process for making a semiconductor integrated circuit device, wherein the delamination of Au wire from the **bonding pad** by interposing an **oxide film** between the **metal layer** and the refractory **metal** silicide **layer**.

L25 ANSWER 12 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:427374 HCAPLUS
DN 131:81421
TI Multilayer electric circuit boards
IN Yoneda, Chikashi
PA Kyocera Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11186434	A2	19990709	JP 1997-349117	19971218

AB The title circuit boards comprise a substrate, alternately laminated multilayer with org. polymer **insulator layers** and thin film circuit layers, conductor-plugged through holes in the **insulator layers** to connect circuit layers each other, and **bonding pads** provided on the upper-most circuit layer so as to connect to external components. The **bonding pads** are coated with Co, Ta, Mo, W, Pd, and/or Pt. The use of the coating materials makes use of thin film circuit layers possible for connection to external components.

L25 ANSWER 13 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:790408 HCAPLUS
DN 130:59885
TI Semiconductor device having a multilayer interconnection structure
IN Ito, Kazunori; Irinoda, Mitsugu; Ueno, Kaichi; Ishida, Mamoru; Kuroda, Takahiko
PA Ricoh Company, Ltd., Japan
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5847466	A	19981208	US 1996-759441	19961205
JP 09219451	A2	19970819	JP 1996-106560	19960426
PRAI JP 1995-318923		19951207		
JP 1996-106560		19960426		

AB A semiconductor device having a multilayer interconnection structure includes a substrate having a **metal** interconnect **layer** and .gtoreq.2 **insulator layers** formed 1 on top of another on the substrate. Each **insulator layer** has a **metal** interconnect **layer** including .gtoreq.1 **bonding pad** section. At least 1 via hole filled with an elec. conductive material is provided in each of the **layers** for interconnecting **metal** interconnect **layers**. At least 1 **bonding pad** connecting hole filled with an elec.

conductive material is provided in each of the layers for interconnecting **bonding pad** sections. The **bonding pad** connecting hole is no more than twice as large in diam. as the smallest via hole.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 14 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:576580 HCAPLUS
DN 127:213730
TI Bonding an aluminum wire to an integrated circuit **bond pad**
IN Hsue, Chen-Chiu; Chien, Sun-Chieh; Chen, Anchor; Hong, Gary
PA United Microelectronics Corporation, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5661081	A	19970826	US 1994-316083	19940930
	US 5734200	A	19980331	US 1997-790336	19970128
PRAI	US 1994-316083		19940930		

AB A process is described for manufg. a **bonding pad** adapted for use with an Al wire that resists stresses which would otherwise peel the pad from the substrate. The pad has a polysilicon layer adhered to an **insulating layer** on a semiconductor substrate, an overlying refractory **metal** silicide **layer**, a 2nd polysilicon **layer**, a refractory **metal layer**, and a thick Al alloy **bonding pad**.

L25 ANSWER 15 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:187003 HCAPLUS
DN 126:194046
TI Photodetector element containing a circuit element and its manufacture
IN Yamamoto, Motohiko; Kubo, Masaru
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 25 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 756333	A2	19970129	EP 1996-111862	19960723
	EP 756333	A3	19980610		
	R: DE, FR, NL				
	JP 09097892	A2	19970408	JP 1996-131856	19960527
	US 6127715	A	20001003	US 1996-685676	19960724
PRAI	JP 1995-187266	A	19950724		
	JP 1996-131856	A	19960527		

AB Si3N4 having high humidity resistance is used as a surface-protecting **insulating film** covering a **metal layer**. In a **bonding pad** portion where the **metal layer** is directly exposed, coverage is provided by a corrosion-resistant metal portion consisting of a Ti-W alloy layer and Au layers. In a signal-processing circuit portion, a light-intercepting

structure and interconnections are provided similarly by a Ti-W alloy layer and Au layer. Thus the humidity resistance of the photodetector element is improved, and the Au layer allows direct die-bonding of a laser chip or the like. Further, since the light-intercepting structure and interconnections can be provided in the signal-processing circuit portion simultaneously with the formation of the Au layer for the **bonding pad** portion, the no. of manufg. steps can be reduced.

L25 ANSWER 16 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:548026 HCAPLUS
DN 125:183569
TI Semiconductor integrated circuit having aluminum multilayer wiring and its manufacture
IN Suzuki, Masayasu; Nishihara, Shinji; Sawara, Masashi; Ishida, Shinichi; Abe, Hiromi; Tooda, Sonoko; Uchama, Hiroyuki; Tsugane, Hideaki; Yoshiura, Aimei
PA Hitachi Ltd, Japan; Hitachi Vlsi Eng; Hitachi Micro System Kk
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08191104	A2	19960723	JP 1995-2551	19950111
	JP 2000208520	A2	20000728	JP 2000-49519	19950111
	US 5904556	A	19990518	US 1996-584065	19960111
	US 6300237	B1	20011009	US 1999-245743	19990208
	US 2002019124	A1	20020214	US 2001-933163	20010821
PRAI	JP 1995-2551	A3	19950111		
	US 1996-584065	A1	19960111		
	US 1999-245743	A3	19990208		

AB The circuit has (1) an uppermost wiring comprising a Ti-TiN laminated barrier **metal film** (X), an Al film, and a TiN barrier **metal film** (Y) which are successively deposited and (2) other wirings comprising Al films sandwiched with the 1st barrier metals. The manuf. of the circuit involves (1) formation of the uppermost wiring by depositing an Al film on X, optionally oxidizing the surface of the Al film, and depositing Y directly or via the oxidized film, and (2) formation of other wirings by depositing an Al film on X, followed by successively depositing Ti and TiN films on the Al film directly or via the oxidized layer. The manuf. involves the following steps: (1) depositing X on an elec. **insulating film** having contact holes, (2) depositing a W film, followed by etching back with a F-contg. plasma to remain only inside the contact hole, (3) sputter-etching the surface of X to remove the remaining F, (4) successively depositing an optional Ti barrier metal, Al, and Ti-TiN another laminated barrier metal, and (5) patterning them and X to form a wiring. In the manuf., the deposition of the Al film is carried out through a low-temp. and high sputter-rate process and a high-temp. and low sputter-rate process. The method gave circuits with good step coverage and showed good adhesion between **bonding pads** and wires.

L25 ANSWER 17 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:330637 HCAPLUS
DN 122:94406
TI Formation of semiconductor integrated circuits by opening a hole to passivation films for bonding

IN Nishihara, Shinji; Sawara, Masashi; Kojima, Masayuki; Tanigaki, Yukio; Haruta, Akira; Kawabuchi, Yasushi
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06177200	A2	19940624	JP 1992-329104	19921209

AB The process involves prepg. an **oxide layer** bound between a circuit layer/Al alloy **bonding pad** laminate and a cap film of, e.g., TiW, W, or TiN, (2) forming a passivation film over the cap film, (3) opening a hole to the passivation film for bonding, and (4) selectively removing the cap metal and the **oxide layers** successively for bonding. The process gives the pad surface an improved bonding property.

L25 ANSWER 18 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:313496 HCAPLUS
DN 120:313496
TI **Bonding pad** structure of semiconductor devices
IN Yoshioka, Kentaro
PA Oki Denki Miyagi Kk, Japan; Oki Electric Ind Co Ltd
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05291343	A2	19931105	JP 1992-90719	19920410
US 5357136	A	19941018	US 1993-42401	19930402
PRAI JP 1992-90719		19920410		

AB The **bonding pad** structure is characterized by elec. connection between a conductor layer made of gate electrode material on a field **oxide film** on a semiconductor substrate and a barrier **metal layer** via openings in an **insulating film** on the conductor layer. The barrier **metal layer** of this **bonding pad** structure does not peel off during bonding process.

L25 ANSWER 19 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:643017 HCAPLUS
DN 113:243017
TI Semiconductor device
IN Takamatsu, Akira
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 02144921	A2	19900604	JP 1988-298106	19881128

AB In a semiconductor advice having an interconnection structure from a metal and silicide on the **metal**, an **insulator film**

on the structure, and an opening in the **insulator film** at the **bonding pad** for transmitting external elec. signals, the silicide exposed in the opening is covered with a high-m.p. metal, and the elec. connection to an external terminal is made via the high-m.p. metal. Specifically, the high-m.p. metal may be W, and may have a reflectivity .gtoreq.70%. By having the high-m.p. metal, optical detection of the bonding-pod region is accurately carried out during the manuf. of the semiconductor device. Addnl., the silicide removal step, which has been required for accurate **bonding-pad** detection in a conventional manufg. process, is eliminated to produce a device having superior H2O resistance, productivity, and quality.

L25 ANSWER 20 OF 20 HCAPLUS COPYRIGHT 2002 ACS
AN 1973:103636 HCAPLUS
DN 78:103636
TI Semiconductor device or monolithic integrated circuit with **tungsten** interconnections
IN Shaw, Joseph Michael
PA RCA Corp.
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3714521	A	19730130	US 1971-166012	19710726
	BE 786665	A1	19721116	BE 1972-120205	19720724
	JP 51016317	B4	19760522	JP 1972-74543	19720725
PRAI	US 1971-166012		19710726		

AB To overcome the difficulties in bonding W to wire and to prevent its high-temp. oxidn., W **metalization** is **coated** with Pt where leads are to be attached and the device is sealed by a protective **insulating layer** except at the **bonding pads**.

L27 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:562579 HCAPLUS
TI Method for packaging integrated circuits with elastomer chip carriers
IN Son, Dae Woo; Lee, Youn Soo; Kim, Byung Man
PA Samsung Electronics, Co., Ltd., S. Korea
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6103554	A	20000815	US 1998-219015	19981223
PRAI	KR 1998-290	A	19980108		

AB A semiconductor chip packaging method includes the provision of individual elastomer chip carriers cut from an elastomer sheet having a uniform thickness and smooth, **parallel** surfaces. The elastomer sheet is **mounted** on an adhesive tape held by a fixing member, such as a support ring, and is then divided into individual carriers. The carrier is attached to a circuit interposer, and a semiconductor chip is attached to the carrier. Circuit leads of the interposer are **bonded** to connection **pads** on the chip. The beam lead bonding area is then encapsulated, and conductive bumps are formed on the underside of the package to serve as input/output terminals for the packaged device. Using this method, an number of devices can be packaged simultaneously on a flexible sheet and then separated into individual devices by cutting the sheet between the devices.

US 098297970BP1

Creation date: 12-05-2003
Indexing Officer: DNGUYEN8 - DANH NGUYEN
Team: OIPEBackFileIndexing
Dossier: 09829797

Legal Date: 04-05-2002

No.	Doccode	Number of pages
1	CTNF	9
2	892	1
3	1449	2

Total number of pages: 12

Remarks:

Order of re-scan issued on .....